Real Time implementation of upstream FDMA-PON over an FPGA platform: Results from the EU project FABULOUS

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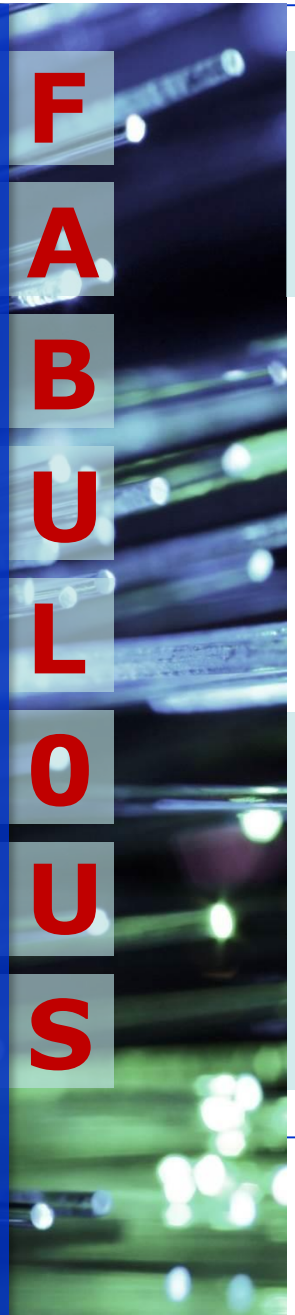
FP7-ICT-2011-8 Challenge 3.5 – STREP project n. 318704 – FABULOUS
FDMA Access By Using Low-cost Optical Network Units in Silicon photonics

FABULOUS at-a-glance



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ILICON PHOTONICS

ARCHITECTURE

SYSTEM PARAMETERS

FP7-ICT-2011-8 – Objective 3.5: Core and disruptive photonic technologies

"Application-specific photonic components and subsystems"

"For access networks, the goal is affordable technology enabling 1-10 Gb/s data-rate per client"

NEW COMPONENTS

The ideas behind the UE STREP "Fabulous"

High capacity

>10Gbps per λ

ITU-T ODN compliant

Future generation

Passive

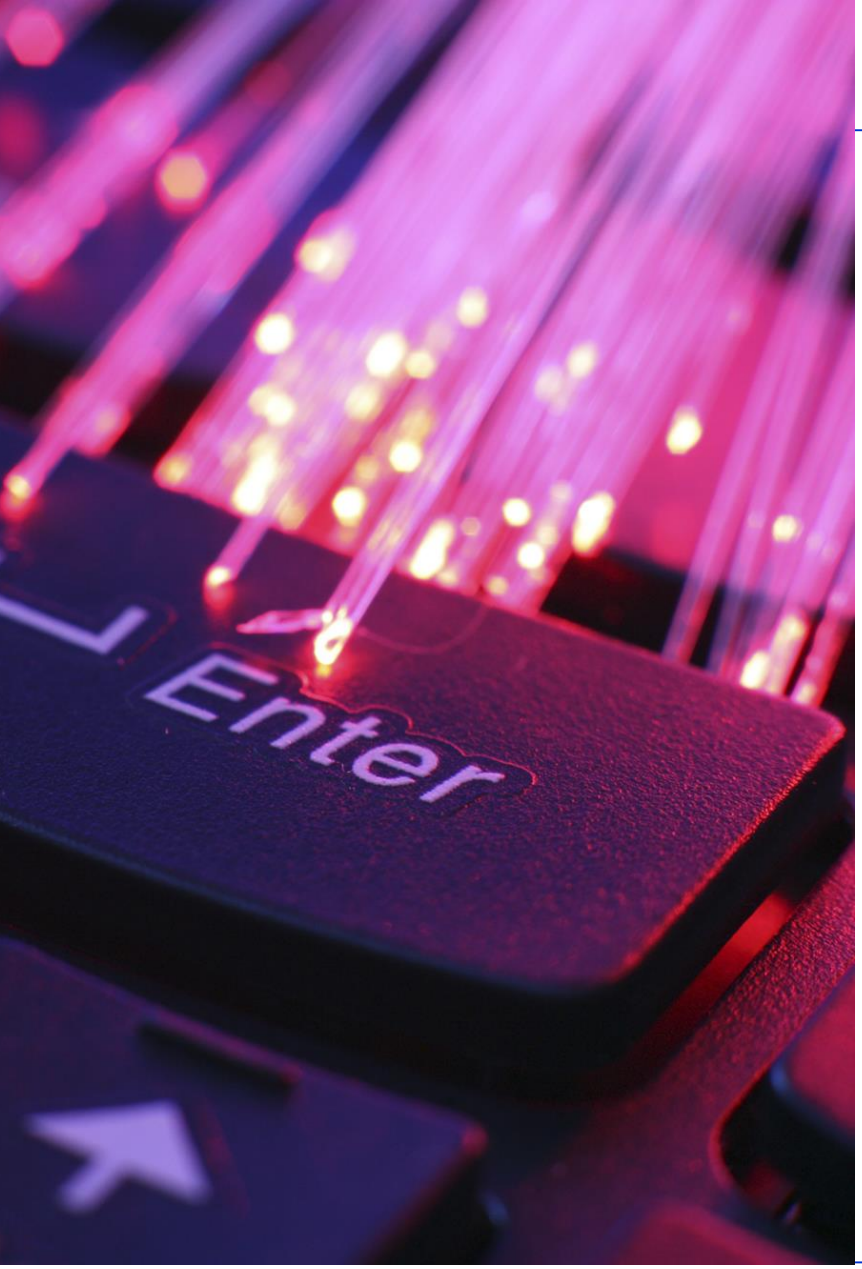
Optical Network

No λ-control at ONU switch-on

High level of optical integration

The research leading to these results has received funding from the European Community's Seventh Framework Programme FP7/2007-2013 under grant agreement n°318704, titled FABULOUS

SELF-COHERENT REFLECTIVE FDMA-PON WITH ONU INTEGRATION ON SiP

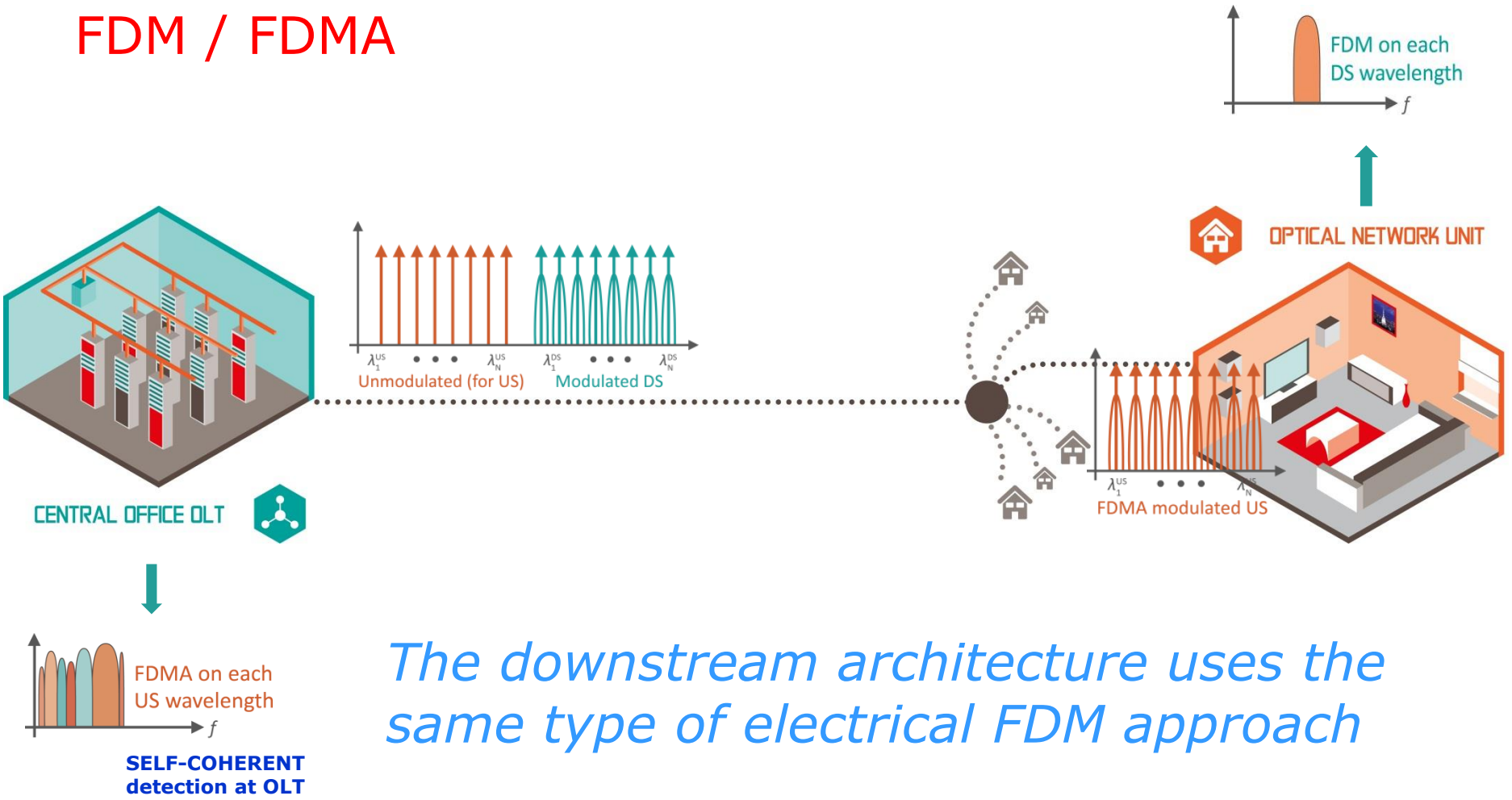


SUMMARY

- **Concept description: architecture and components**
- **FPGA implementation**
- **DSP FPGA implementation**
- **Conclusions**

UPSTREAM ARCHITECTURE

Reflective WDM PON based on FDM / FDMA

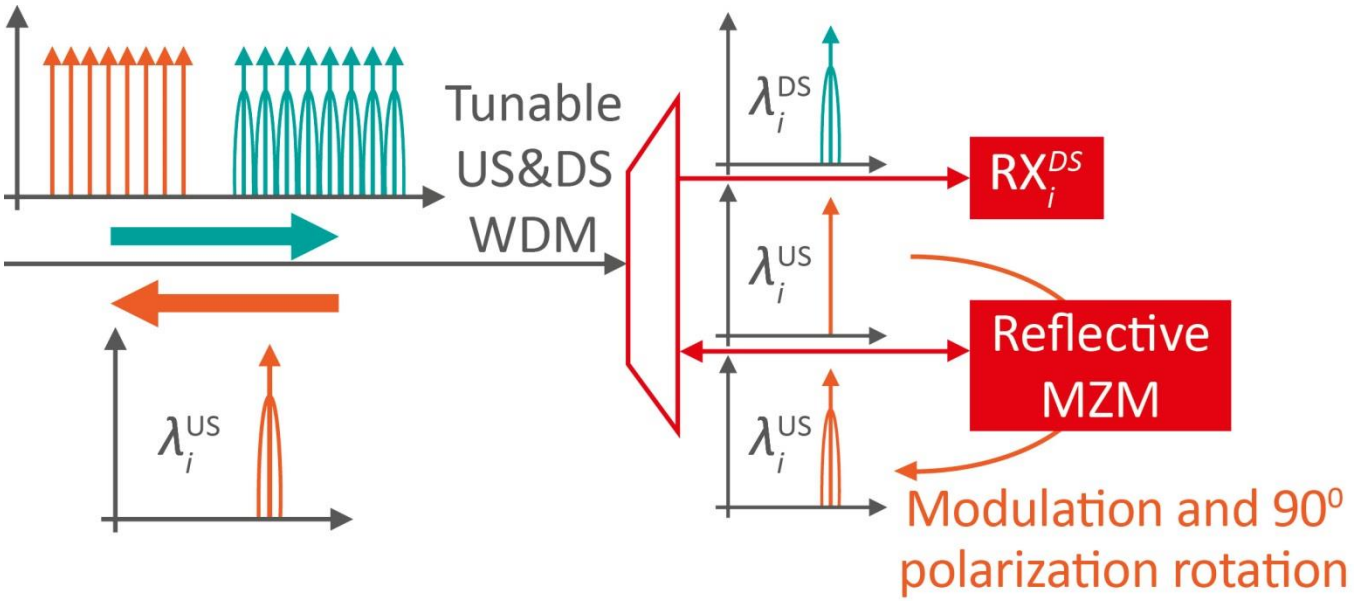


The downstream architecture uses the same type of electrical FDM approach

The ONU photonic chip

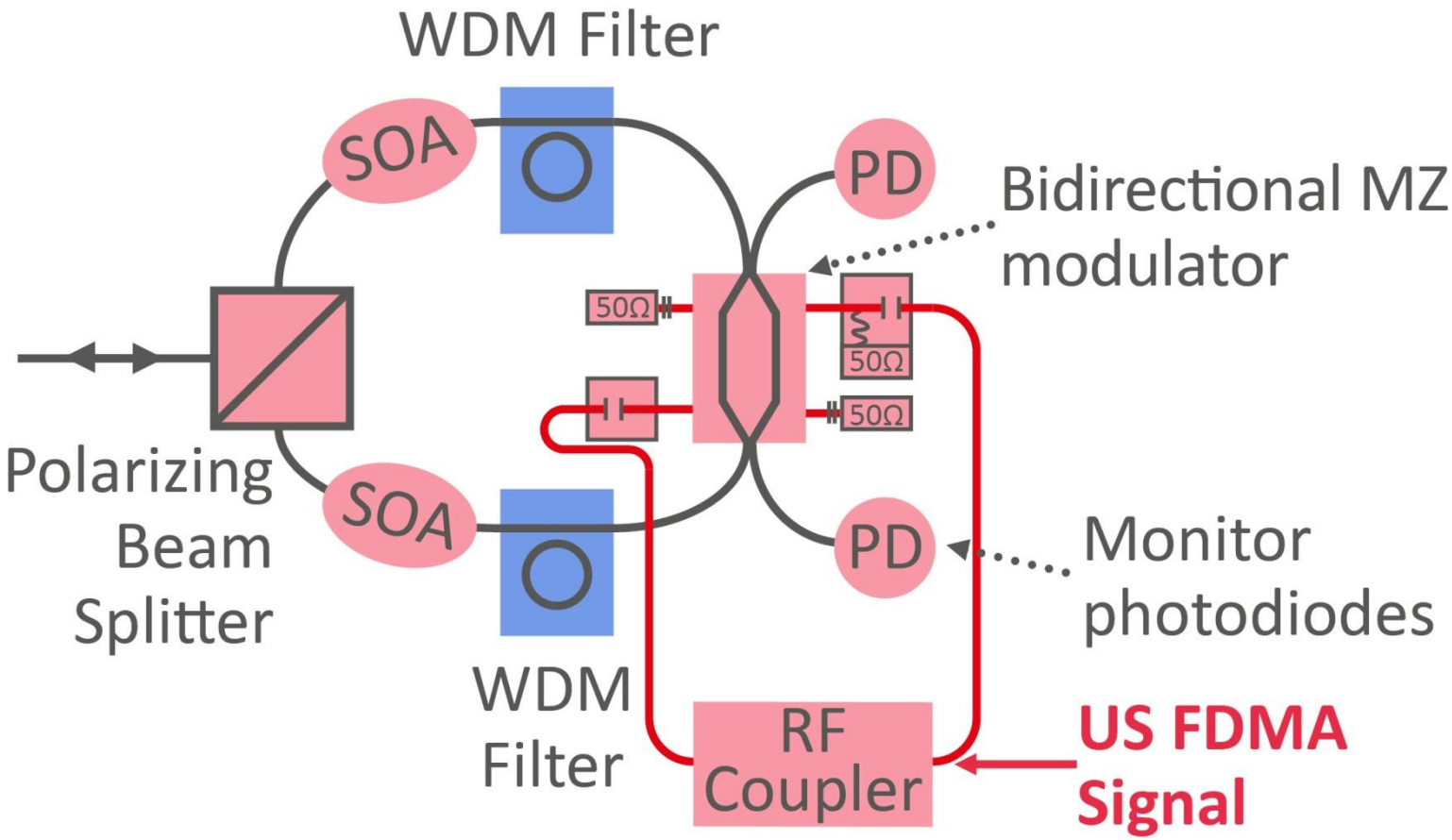
ONU Main functionalities:

- Select the proper US and DS wavelengths
- reflects the seed signal
- modulates it using QAM on the assigned electrical subcarrier (and wavelength)
- performs 90° polarization rotation (Faraday effect)

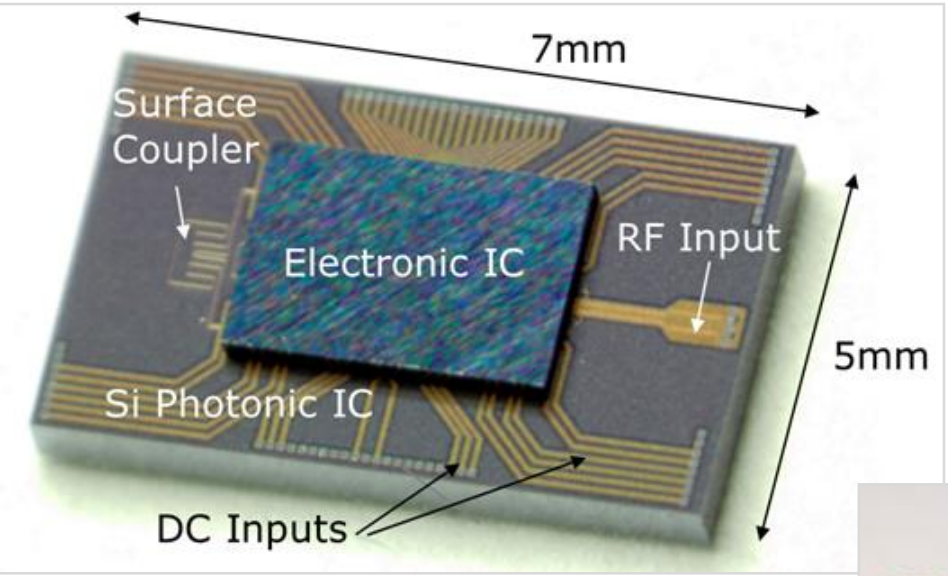


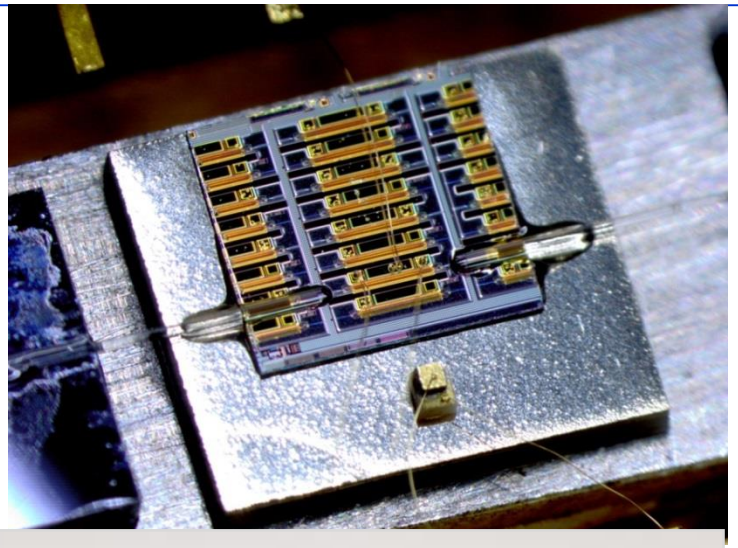
The ONU - details

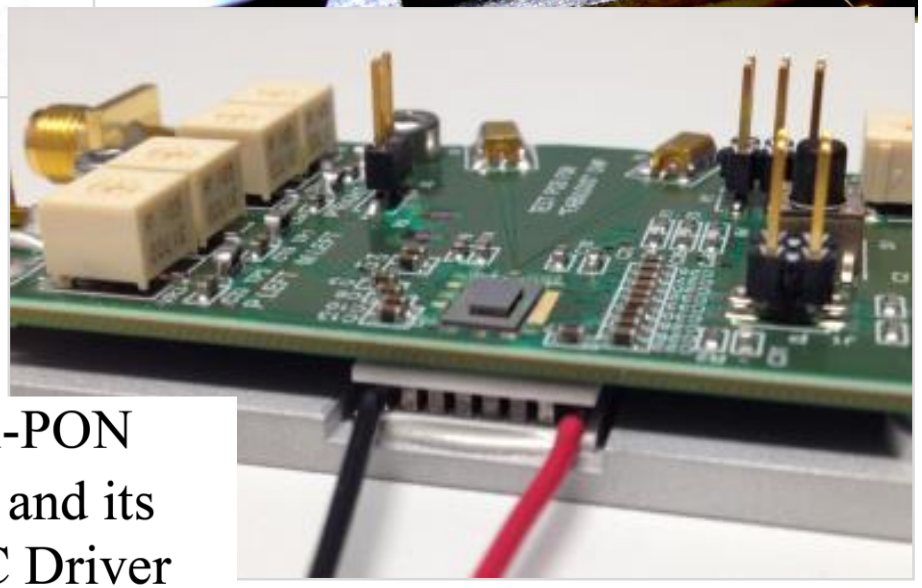
One of the main purpose of the project is to integrate the ONU on a Silicon Photonics PIC



Silicon Photonics PIC





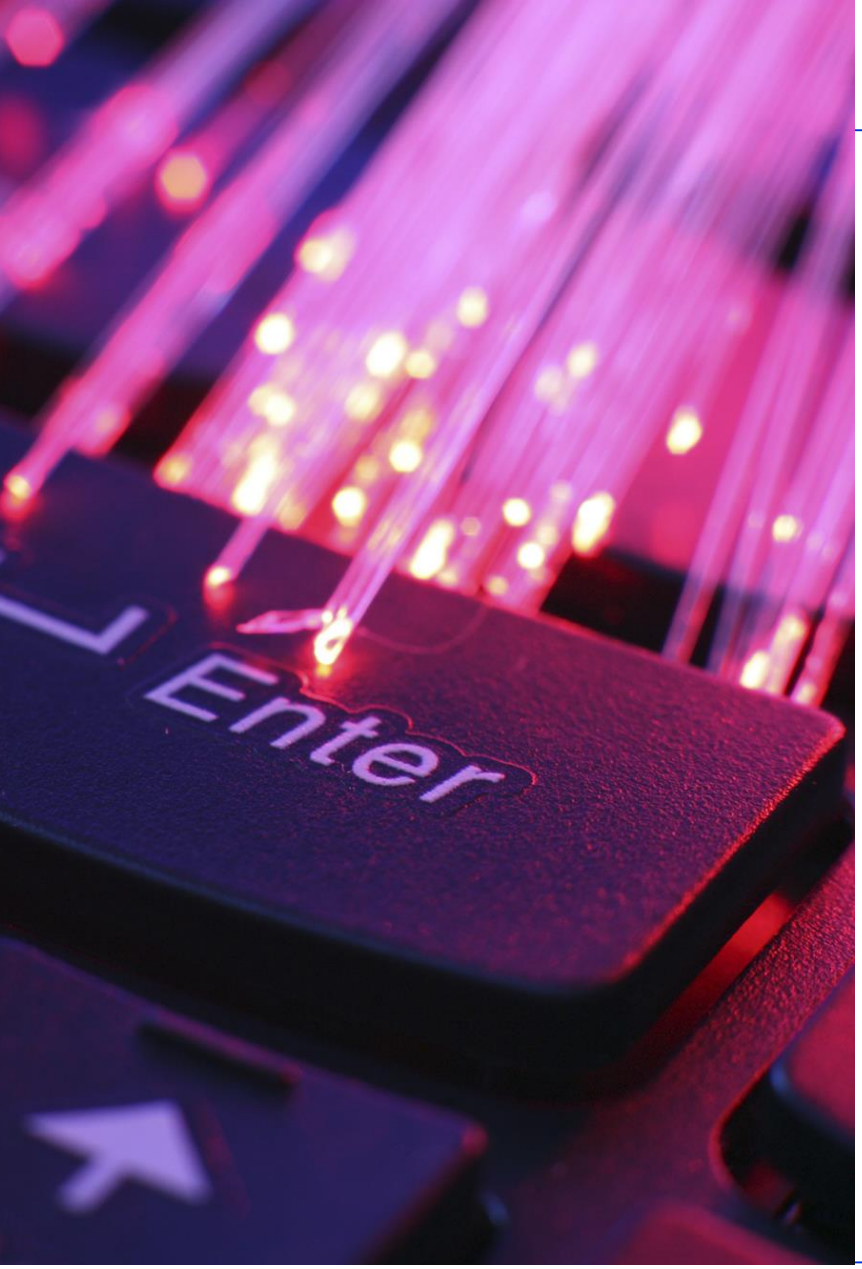


First full-fledged «FABULOUS PIC» released in Spring 2016

16-QAM-Transmitter for FDMA-PON Made up of a Silicon Photonic IC and its Flip-Chipped CMOS Electronic IC Driver

Journal of Lightwave Technology, vol. 34, no. 10, pp. 2391-2397, May15, 15 2016.

Sylvie Menezo, *Member, IEEE*, Enrico Temporiti, Junsu Lee, Olivier Dubray, Stéphane Bernabé, *Member, IEEE*, Daniele Baldi, Gabriele Minoia, Matteo Repossi, André Myko, Sonia Messaoudène, Maryse Fournier, Lee Carroll, Silvio Abrate, *Member, IEEE*, Roberto Gaudino, *Senior Member, IEEE*, Peter O'Brien, and Benoit Charbonnier



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Where did we start from?

1Gbps net data rate per user (symmetrical) using:

- 1.2 Gbps gross data rate including all overheads
- 16-QAM on each subcarrier at approx. 300 Mbaud
- Raised-cosine filtering with 0.1 roll-off
- Electrical subcarrier spaced at 330 MHz (no guardbands needed)

Off-line processing experiments for both US and DS demonstrated **32 Gbps aggregated** rate per wavelength

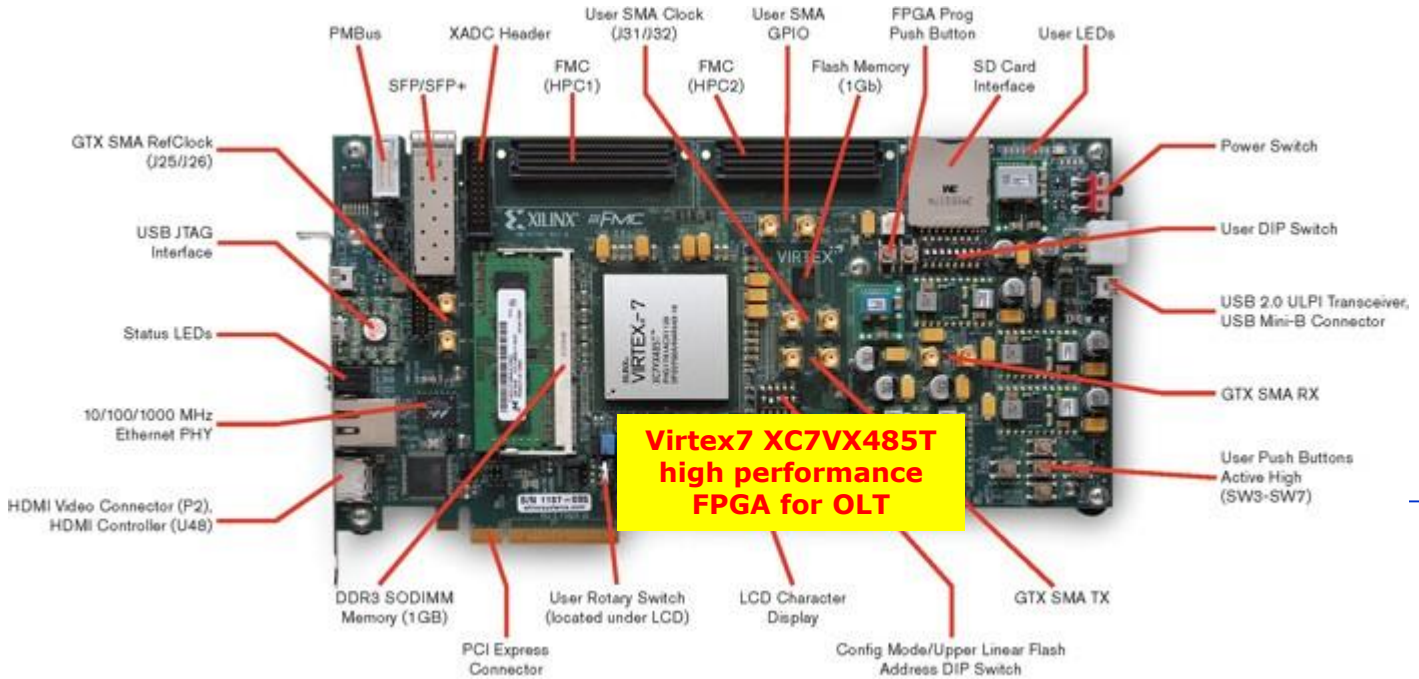
Overview of the FABULOUS EU Project: Final System Performance Assessment With Discrete Components

Silvio Abrate, *Senior Member, IEEE*, Stefano Straullu, Antonino Nespola, Paolo Savio, Joana Chang, Valter Ferrero, Benoit Charbonnier, and Roberto Gaudino, *Senior Member, IEEE*

(Invited Paper)
JOURNAL OF LIGHTWAVE TECHNOLOGY, VOL. 34, NO. 2, JANUARY 15, 2016

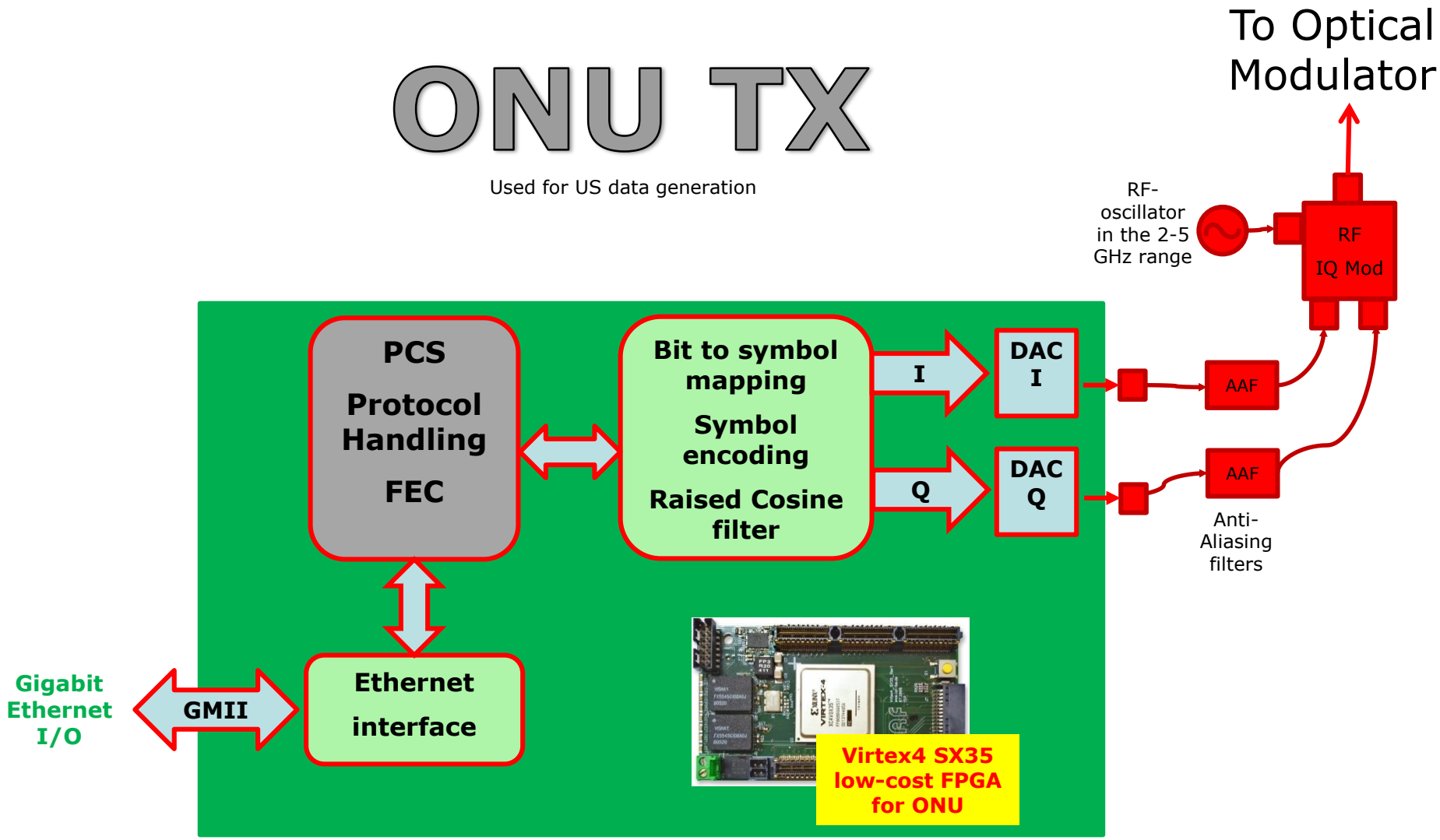
FPGA implementation

- ADC and DAC running at 1200 Msample/s
- Parallel bus of 4 samples per symbol on both FPGAs (US and DS)
- Finite math
- Latency (pipeline registers)



SEVENTH FRAMEWORK PROGRAMME

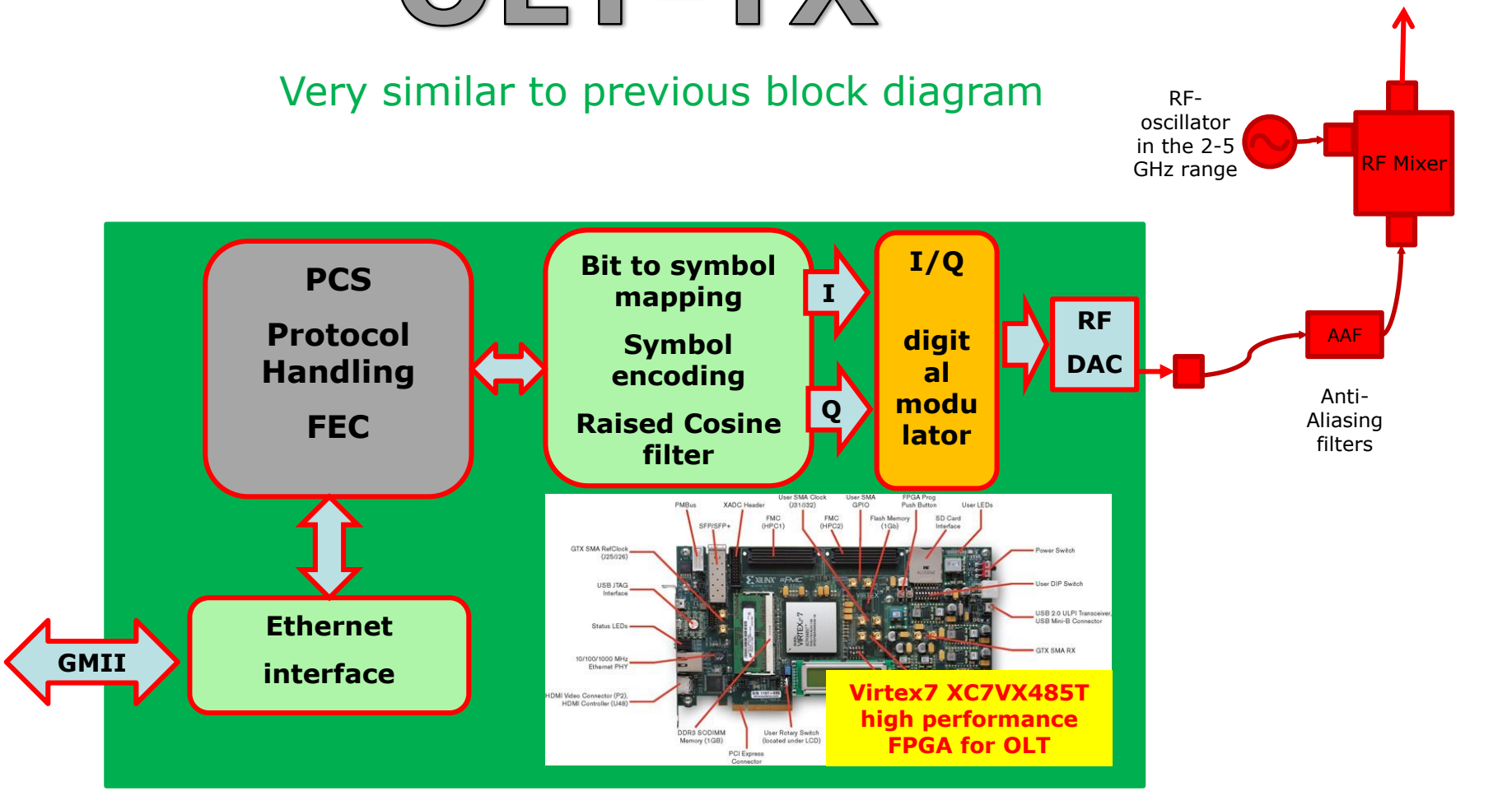
ONU TX block diagram



OLT TX block diagram

OLT-TX

Very similar to previous block diagram



OLT self-coherent receiver DSP

coherent receiver front end

A D C

12 bit

Blind Adaptive Equalizer, CMA approach

Feed Forward Filter

Error block

Taps Updating block

Modified Viterbi-Viterbi CPE

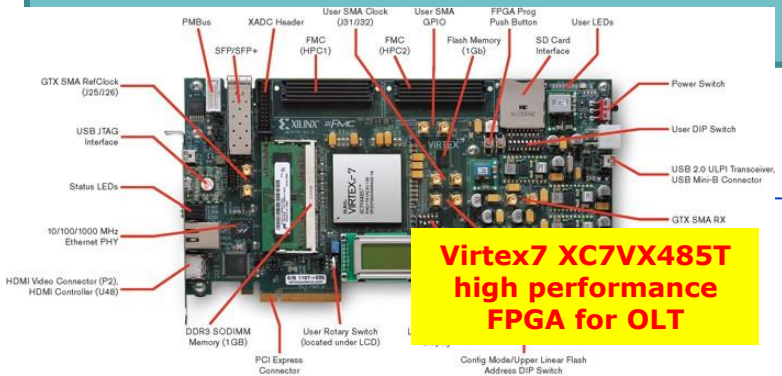
Carrier Phase Estimation

Decisor

Differential Decoder

Symbol to Bit de-mapping

Physical Coding Sublayer



Virtex7 XC7VX485T high performance FPGA for OLT

SEVENTH FRAMEWORK PROGRAMME

OLT RX Main blocks

Virtex4 SX35 low-cost FPGA for ONU

OLT

ADC

Complex data

Blind Adaptive Equalizer

Feed Forward Filter

Error block

dating

Scatter plot

Quadrature

In-Phase

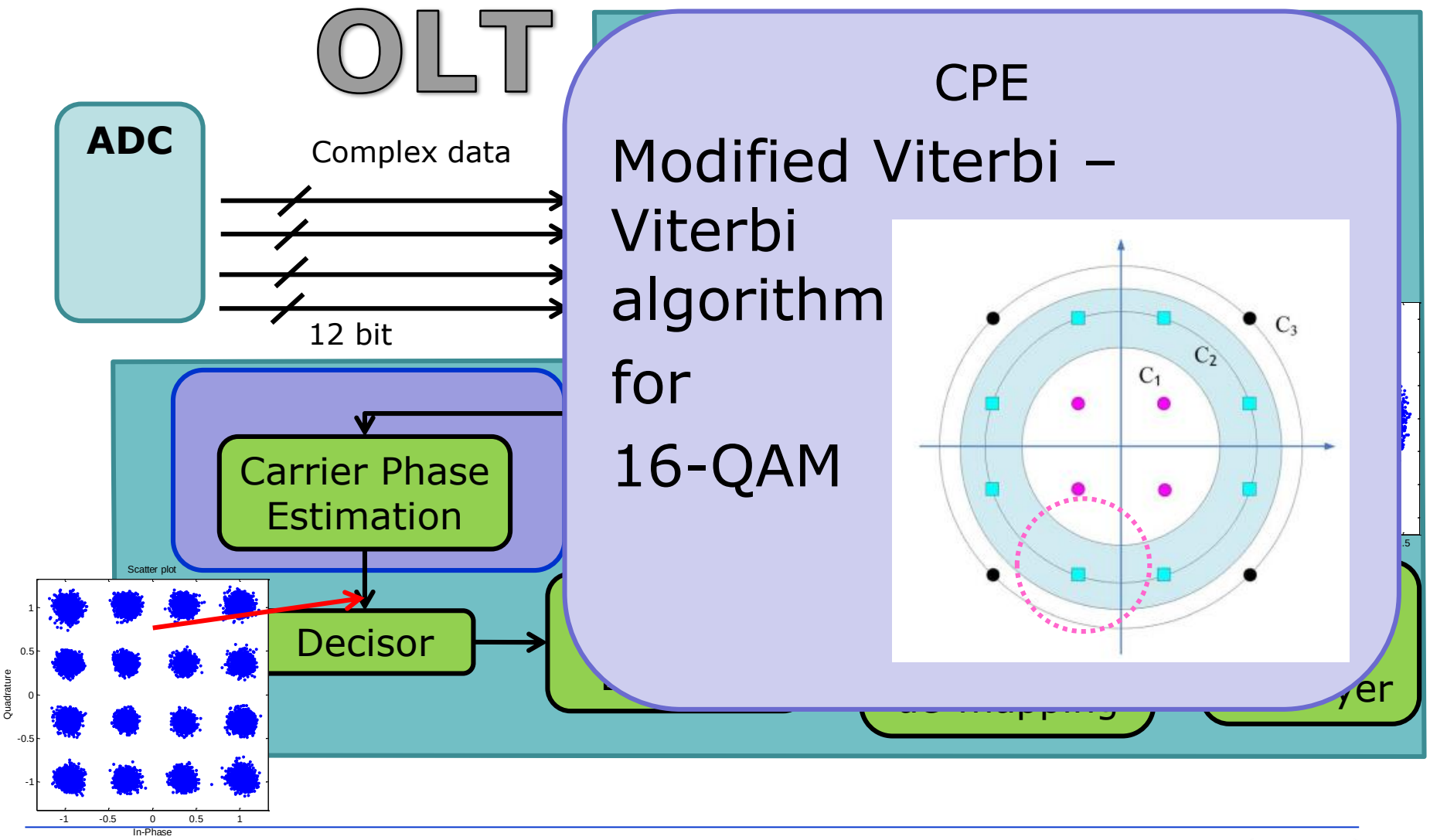
Symbol to Bit de-mapping

Physical Coding Sublayer

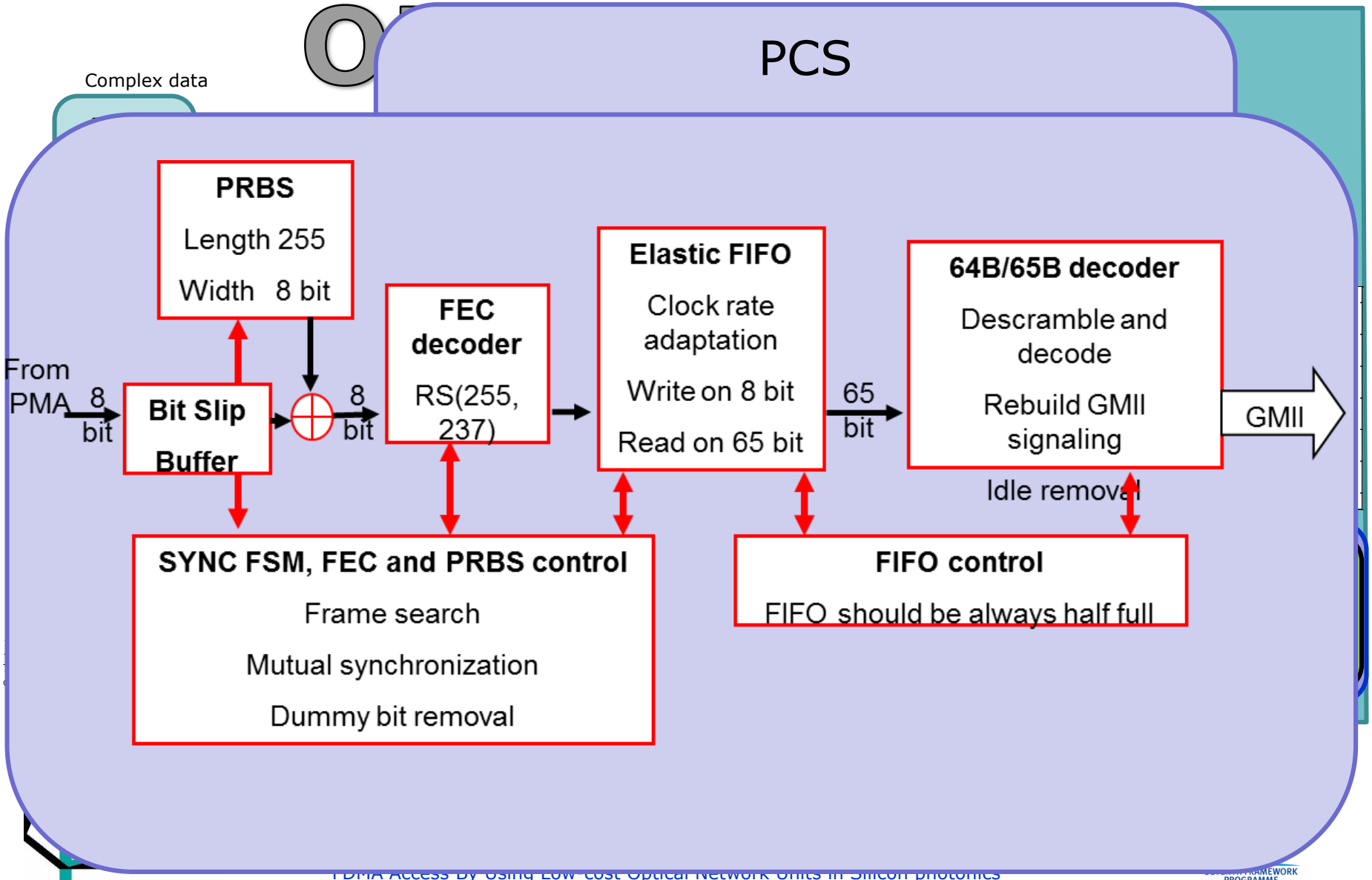
EQUALIZER

- 4 to 1 downsampling filter
- 64 complex taps (16 symbols)
- Delayed Block LMS tap update algorithm:
  - Constant Modulus Algorithm (CMA)
  - Radius Direct Equalizer (RDE)

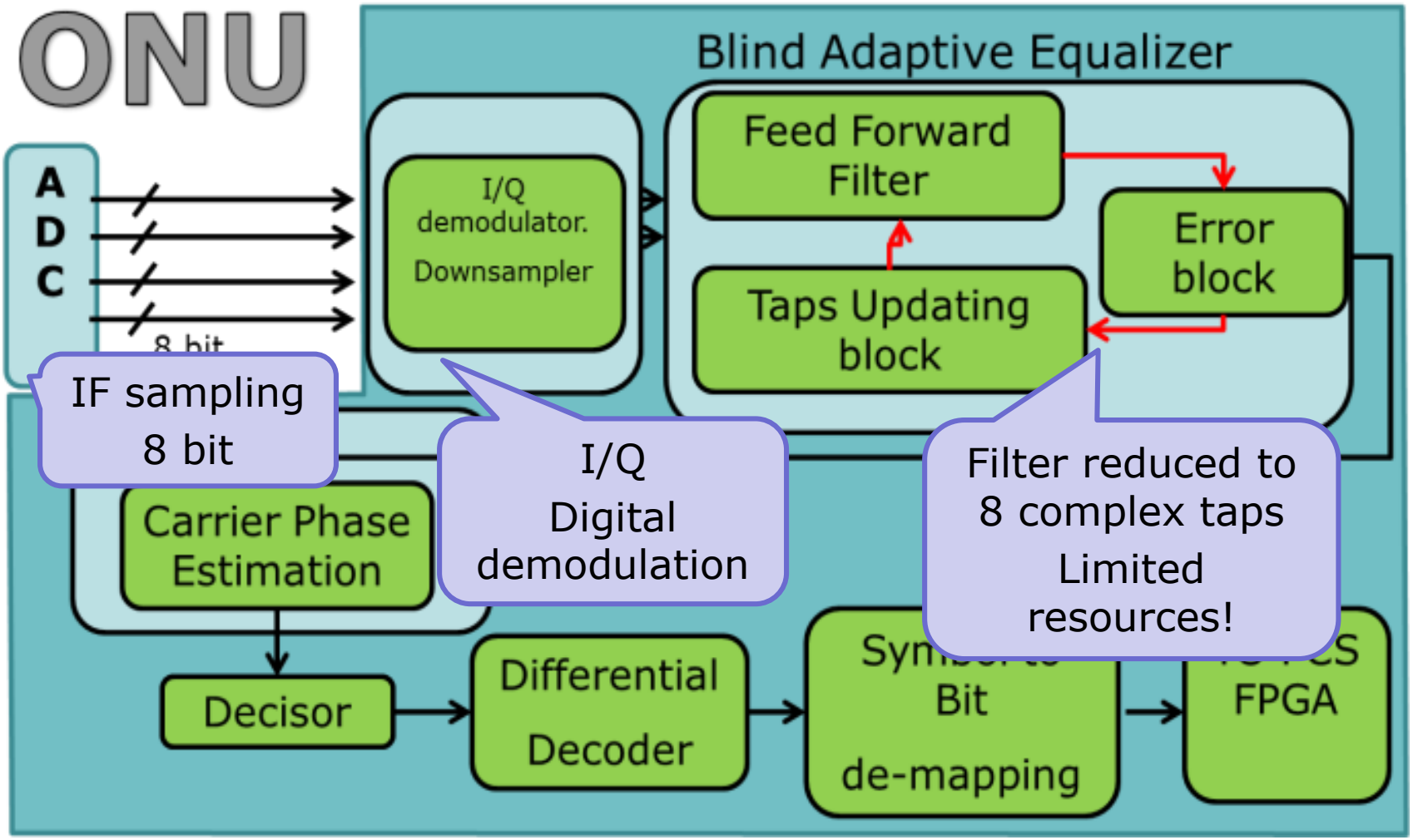
OLT RX Main blocks



OLT RX Main blocks



ONU RX


ONU
Blind Adaptive Equalizer
A
D
C
8 bit
I/Q
demodulator.
Downsampler
Feed Forward
Filter
Error
block
Taps Updating
block
IF sampling
8 bit
I/Q
Digital
demodulation
Filter reduced to
8 complex taps
Limited
resources!
Carrier Phase
Estimation
Decisor
Differential
Decoder
Bit
de-mapping
FPGA

ASIC Size and Power Consumption Estimation

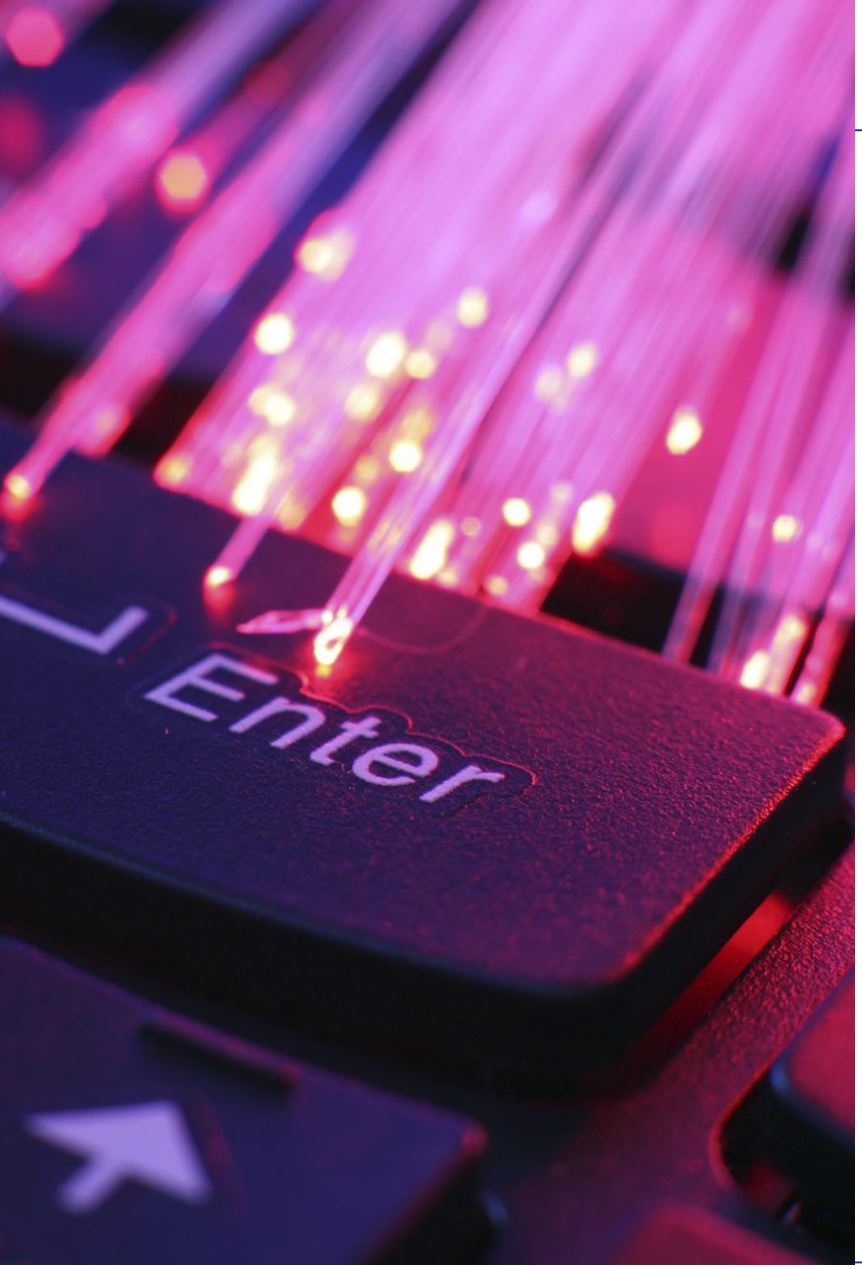
For the DS receiver section, the ONU chip should include:

- a two channel 600 MHz ADC;
- an adaptive low-pass down-sampling filter, implemented as a FIR filter with 32 complex taps;
- the CPE;
- the differential decoder;
- a FEC decoder based on ITU G.975 I.4 EFEC.

For the US section, our analysis considered three main blocks:

- a FEC encoder using a 20.5% overhead FEC.
- a SRRC up-sampling filter, made of 128 complex taps;
- a dual 600 MSps DAC.

On a 65nm CMOS process, estimated total area is 7mm^2 and power consumption <4,2W



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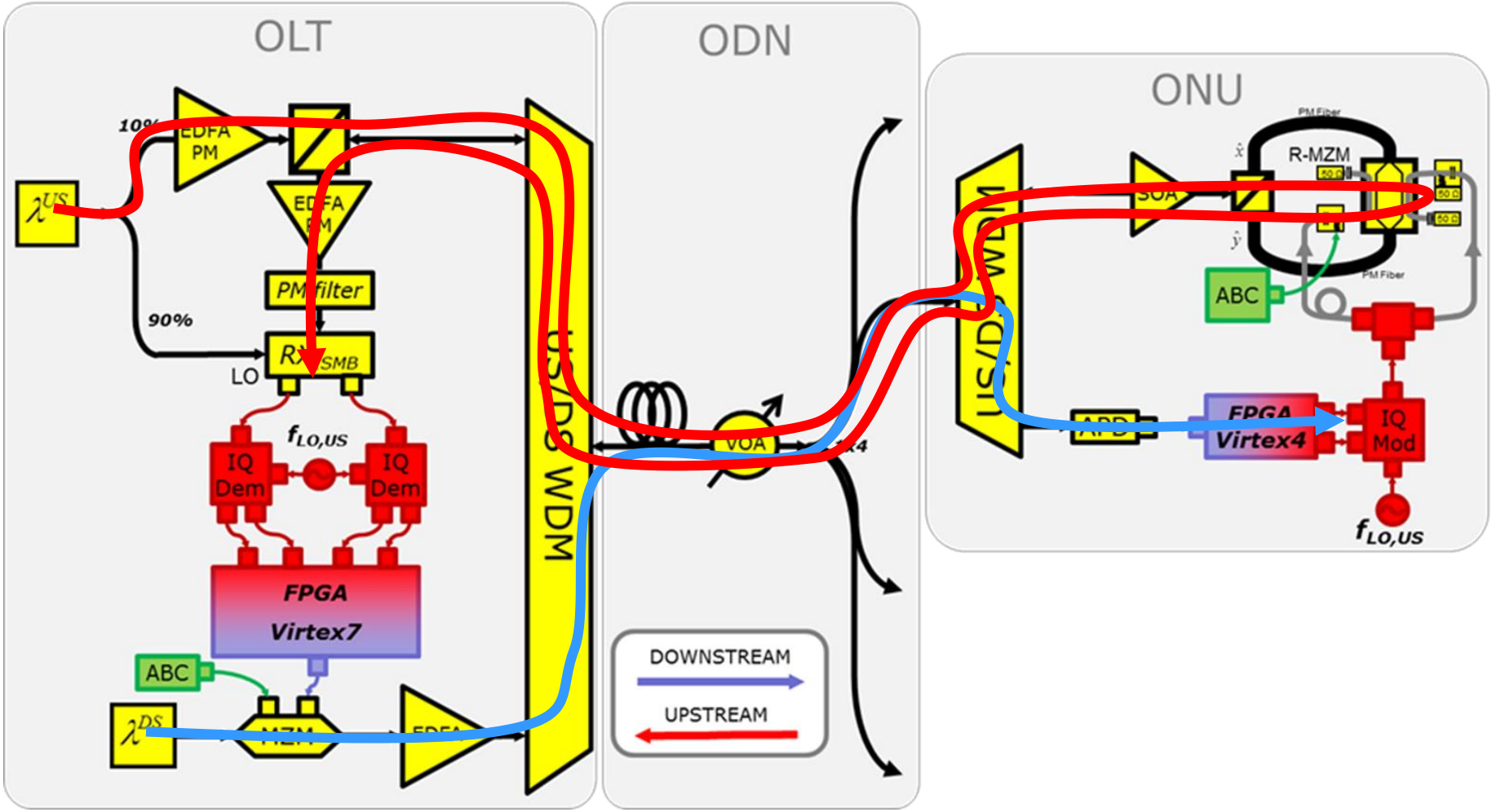
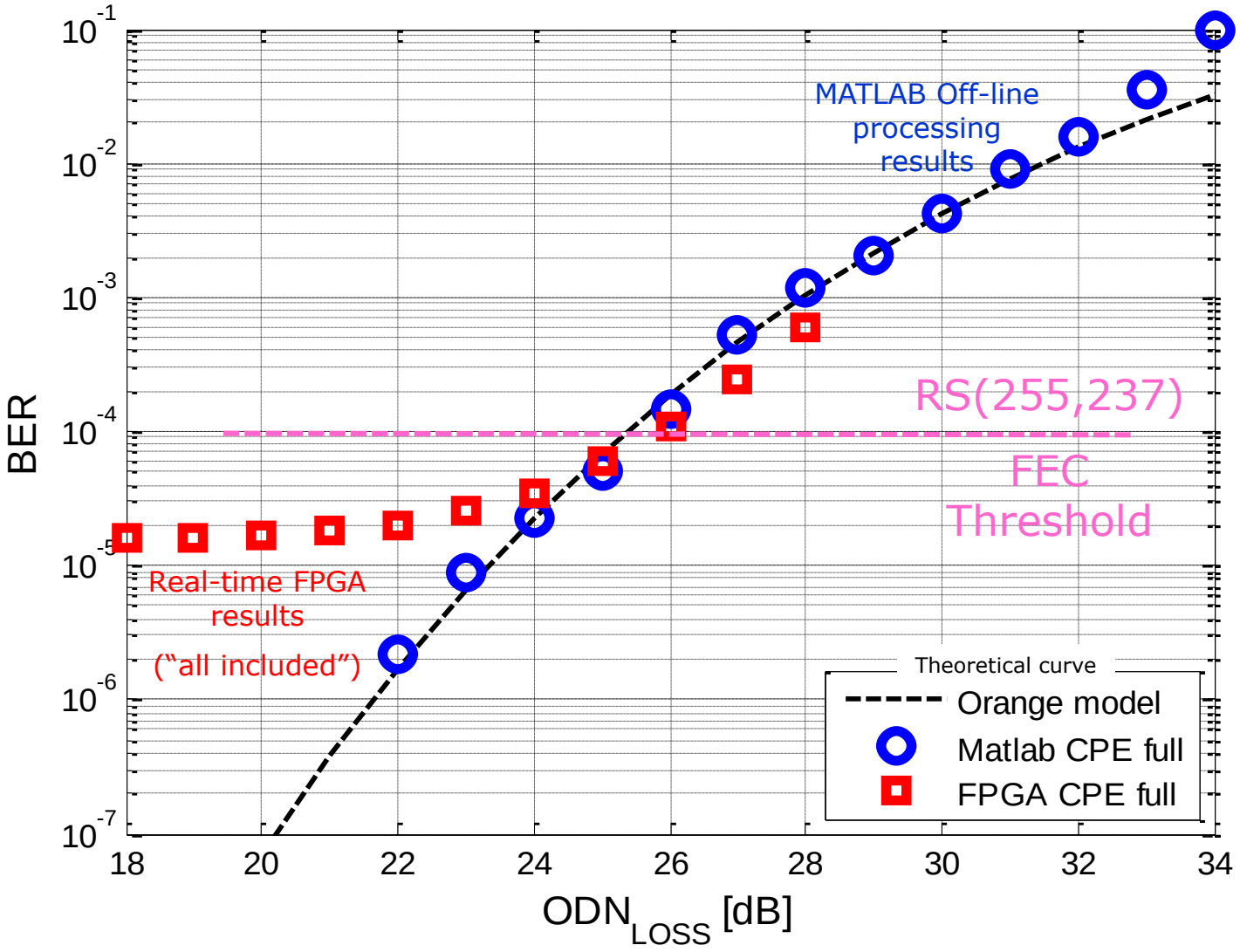
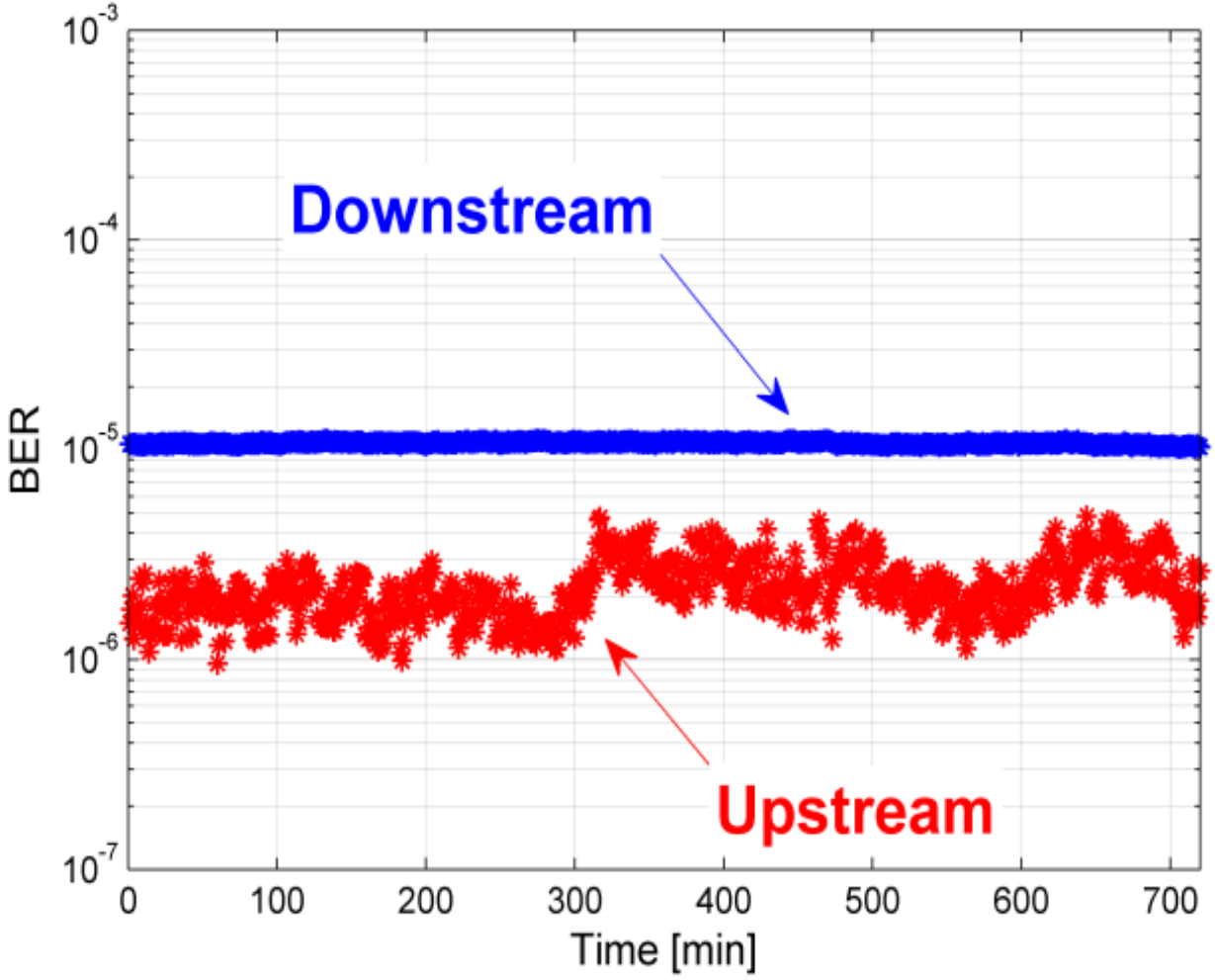
Full bidirectional system

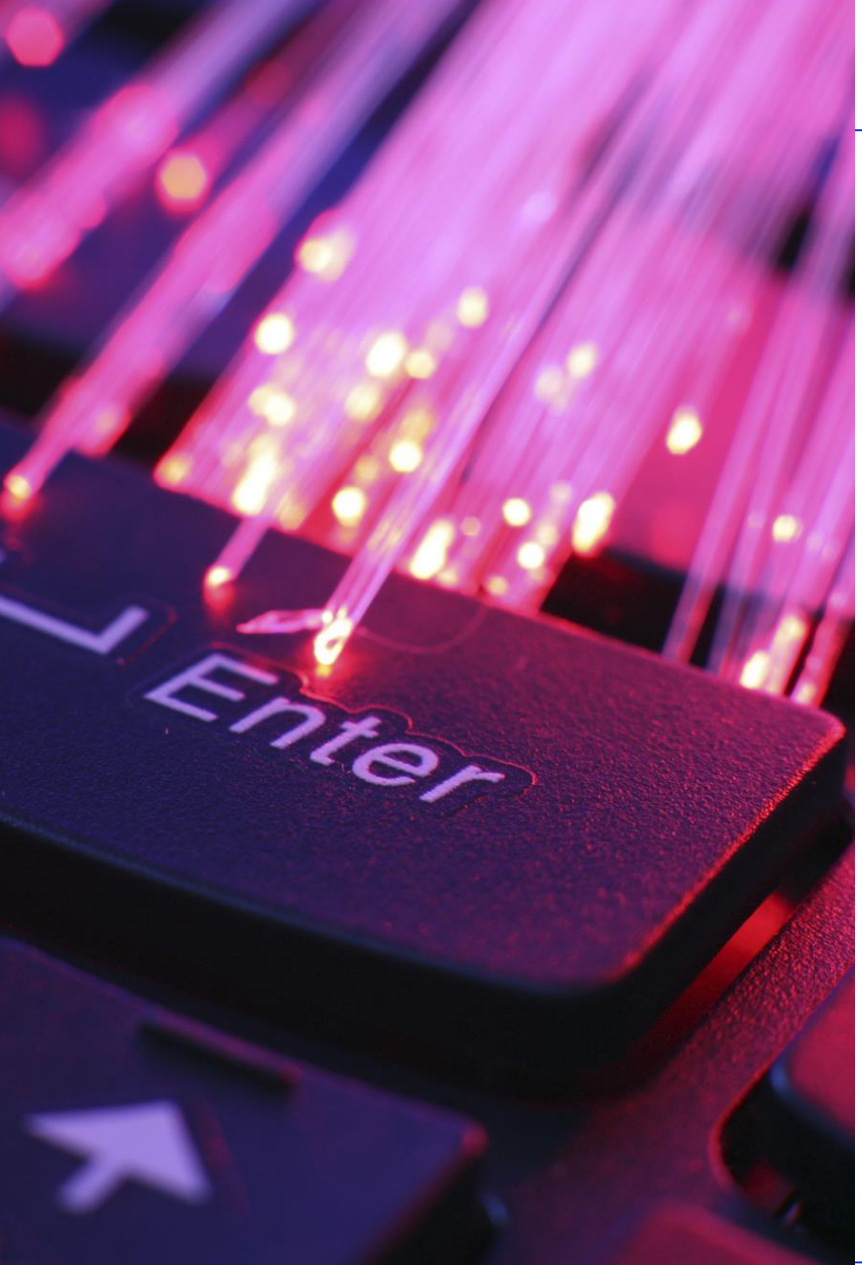


Results for upstream coherent receiver



Long term BER results (11 hours)





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Conclusions

We have presented the first results of real time data transmission on Fabulous upstream and downstream channels

The real time results compare well with theoretical and off-line DSP results.

We are still investigating the floor present in our real time experiments

Acknowledgments

The research leading to these results has received funding from the European Community's Seventh Framework Programme FP7/2007-2013 under grant agreement n°318704, titled:

FABULOUS: "FDMA Access By Using Low-cost Optical Network Units in Silicon Photonics"

WEB site: www.fabulous-project.eu

To contact the coordinator: info@fabulous-project.eu

To contact the author: roberto.gaudino@polito.it

The OLT

Polarization rotation allows simplified coherent detection at the OLT