Demonstration of upstream WDM+FDMA PON and real time implementation on an FPGA platform

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FDMA Access By Using Low-cost Optical Network Units in Silicon photonics

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FABULOUS: "FDMA Access By Using Low-cost Optical Network Units in Silicon Photonics"

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Presentation outline

- The EU FABULOUS architecture at a glance
  - Upstream, self-coherent, reflective FDMA-PON
- The WDM transmission experiments
  - FDMA on top of 4 wavelengths WDM
- The DSP real time implementation on an FPGA platform
  - Full protocol implemented for upstream transmission

FABULOUS at-a-glance

FDMA
ACCESS
BY
USING
LOW-COST
OPTICAL NETWORK
UNITS IN
SILICON PHOTONICS

ARCHITECTURE

SYSTEM PARAMETERS

This part is almost over after 2.5 years of work inside the EU project.

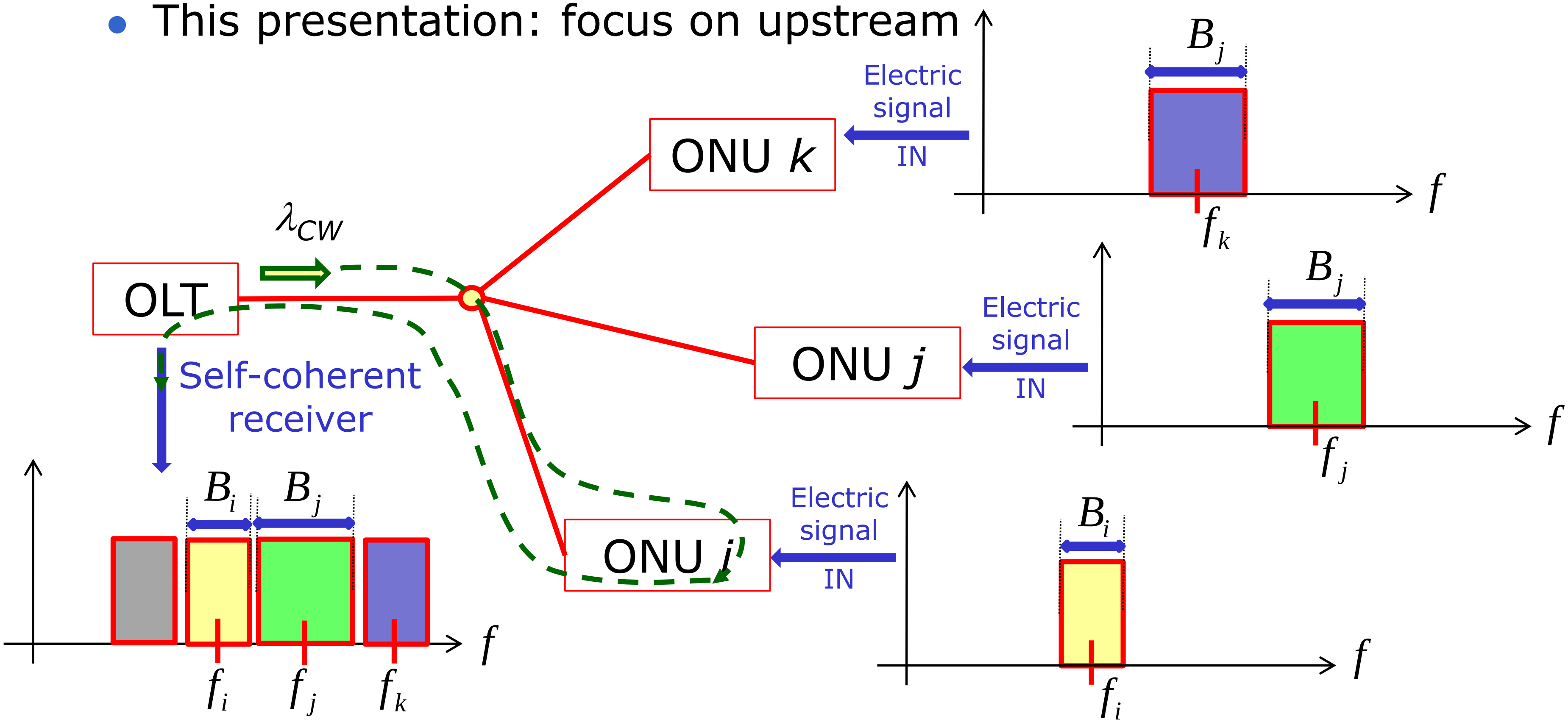
This presentation is a “final” presentation on the System workpackage of the project

NEW integrated optoelectronic COMPONENTS for the ONU

SEVENTH FRAMEWORK PROGRAMME

Upstream FDMA-PON architecture

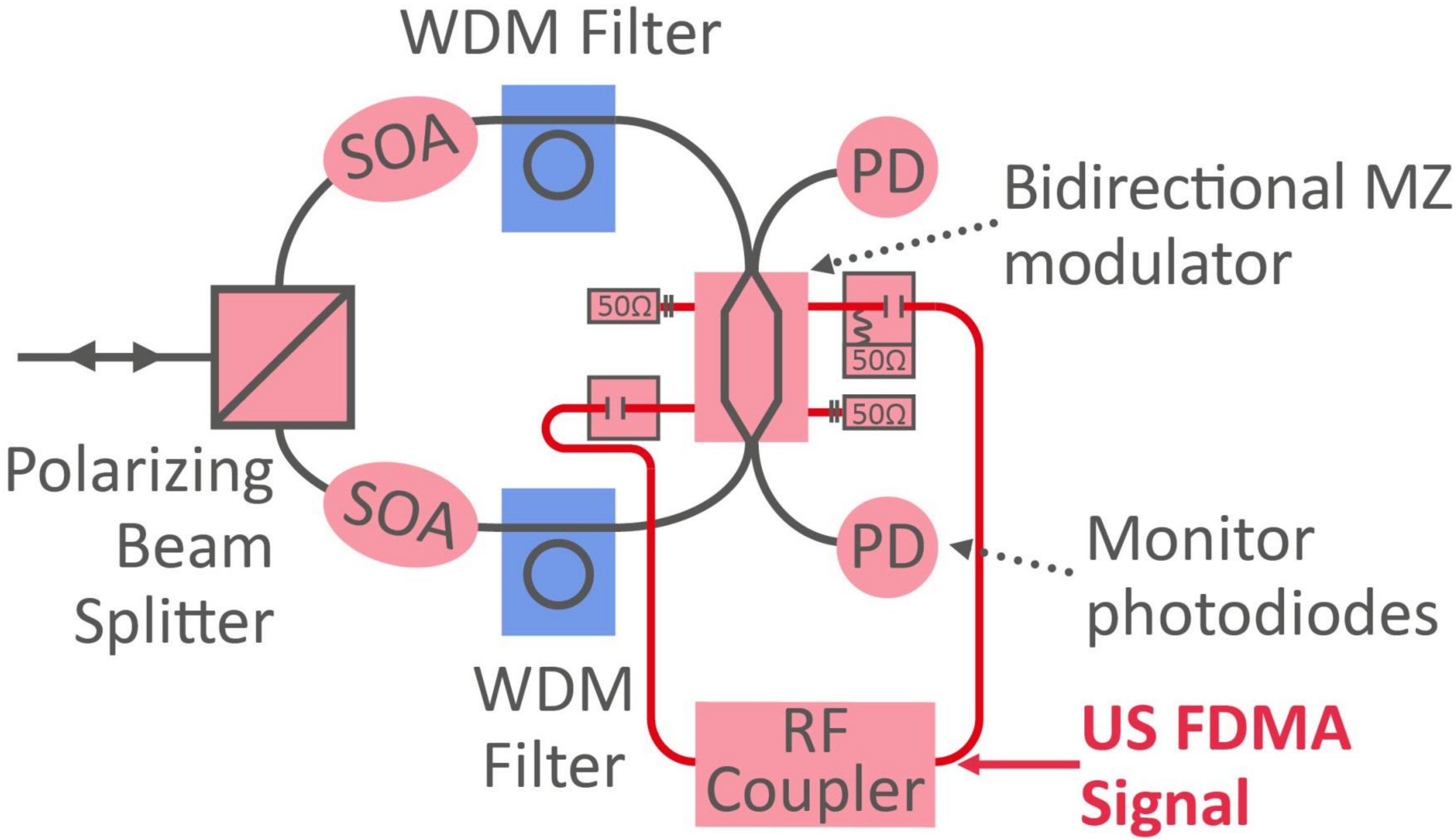
- PON based on electrical subcarrier FDM/FDMA in both directions
  - "standard" Optical Distribution Network (ODN)
    - ➔ 1x64 splitter-based ODN
  - This presentation: focus on upstream



The ONU

The ONU reflects the CW seed signal and modulates it using M-QAM + FDMA approach

One of the goals of the project is to integrate the ONU using a Silicon Photonics PIC



Best result so far for UPSTREAM transmission

(Invited paper at OFC 2015)

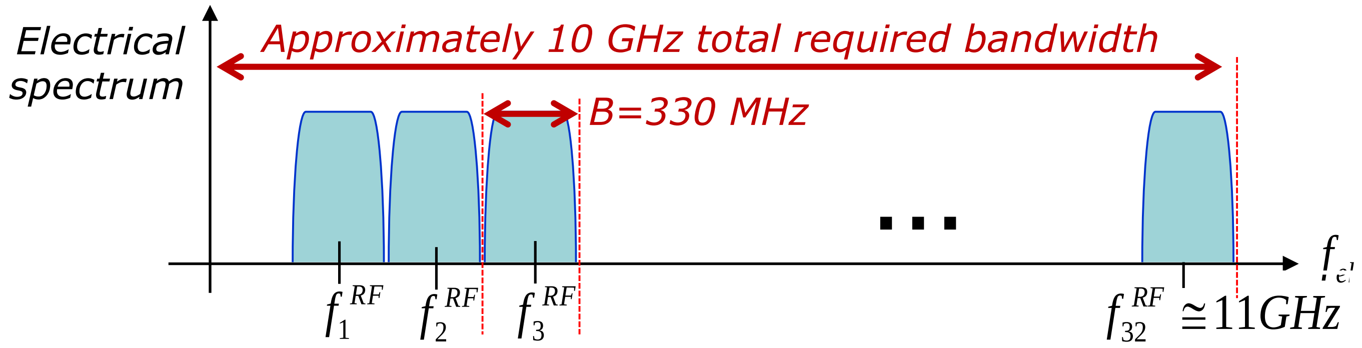
DATA RATE PER USER SET AT 1 GBPS

- net data rate, giving a gross rate of 1.2 Gbps including FEC, overhead and line coding

MODULATION FORMAT SET AT 16-QAM using electrical subcarriers

- Requires *B*~330 MHz per user
  - Using Raised cosine spectrum, roll-off=0.1

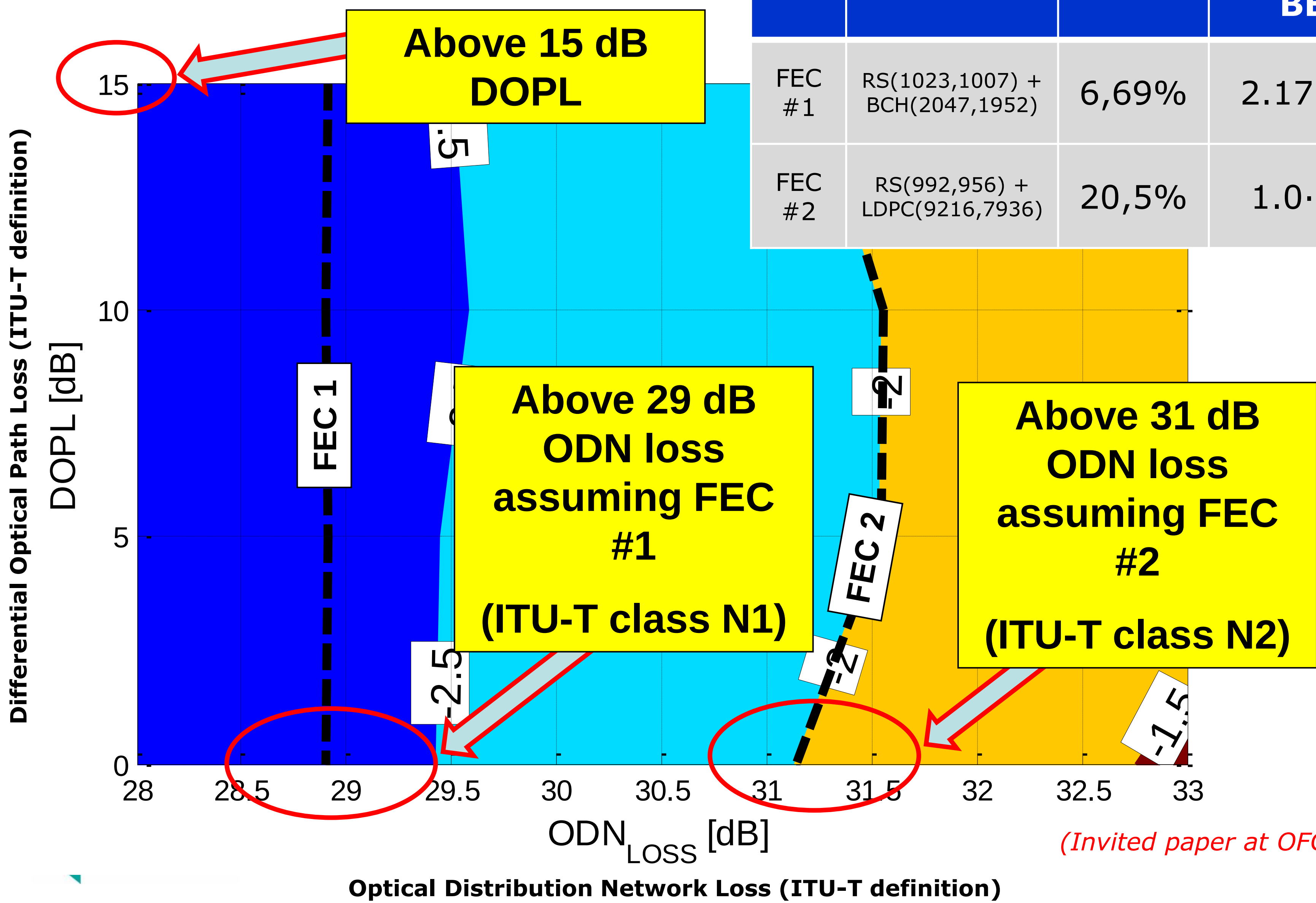
32 USERS PER WAVELENGTH on the 11 GHz available electrical band → **32 Gbit/s upstream capacity on a single λ**



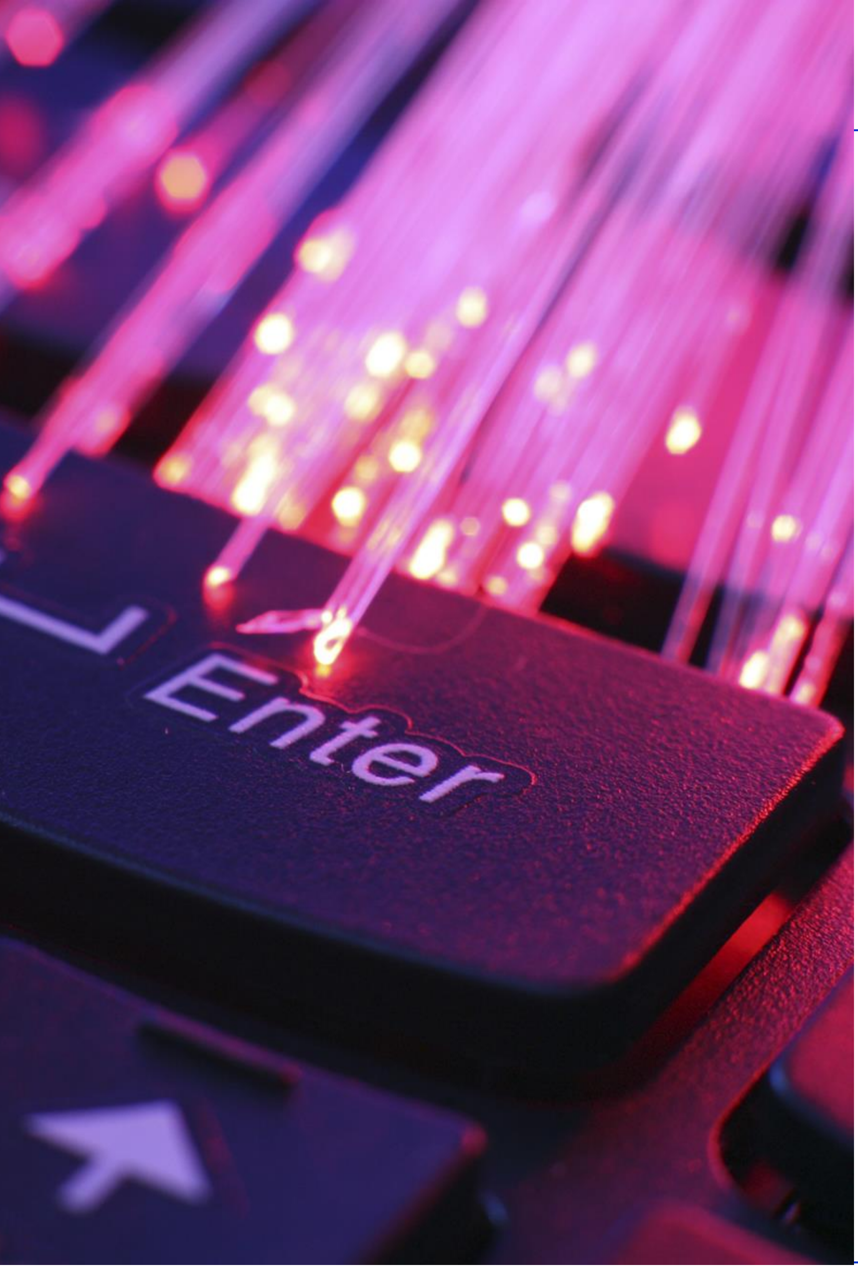
Results using discrete optoelectronic components

BER contour plots

FEC	Code	Overhead	pre-FEC BER
FEC #1	RS(1023,1007) + BCH(2047,1952)	6,69%	$2.17\cdot10^{-3}$
FEC #2	RS(992,956) + LDPC(9216,7936)	20,5%	$1.0\cdot10^{-2}$



(Invited paper at OFC 2015)



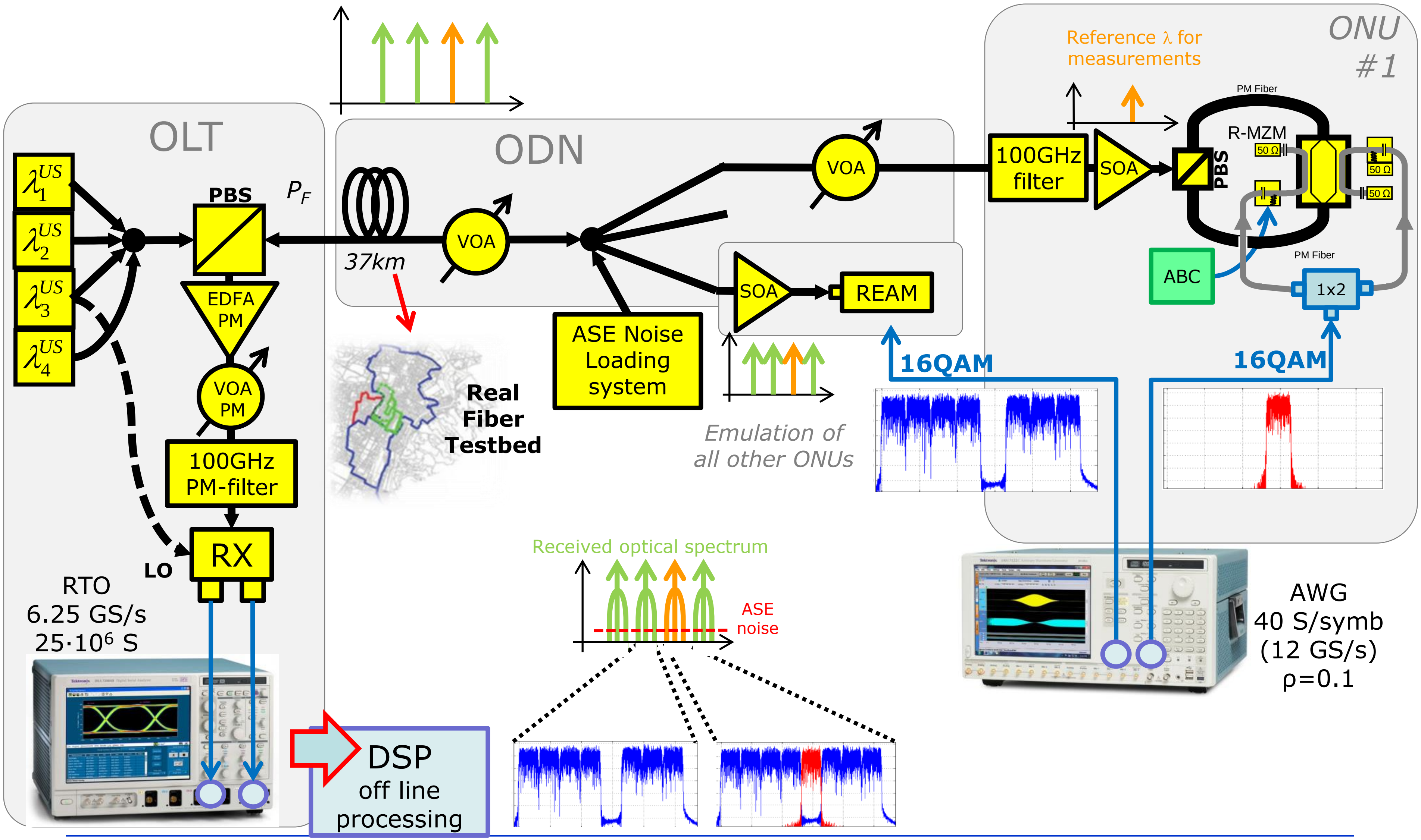
WDM Experiments

on upstream, using discrete optoelectronic components

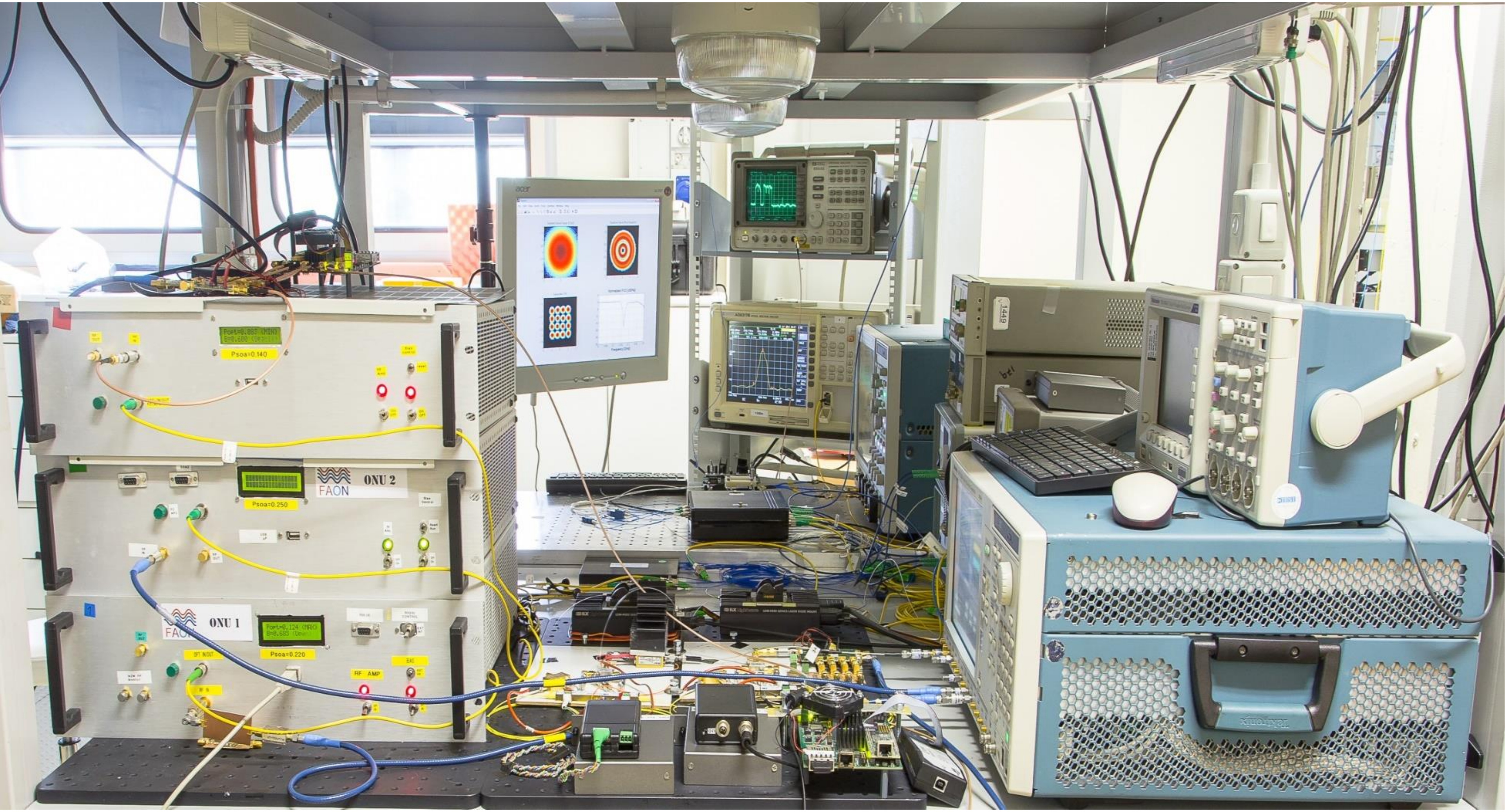
4 λ WDM setup, NET bitrate per ONU= 1Gbps

- We used 4 wavelengths on a 100 GHz grid
  - Similarly to what is set for TWDM-PON in NG-PON2 ITU-T G.989
- We wanted to check if WDM introduced significant impairments
  - We focused again only on upstream
  - On each wavelength: same 16-QAM over electrical FDMA approach as in OFC2015
- We thus transmitted <u>4x32=128 Gbit/s</u> (net) for upstream transmission

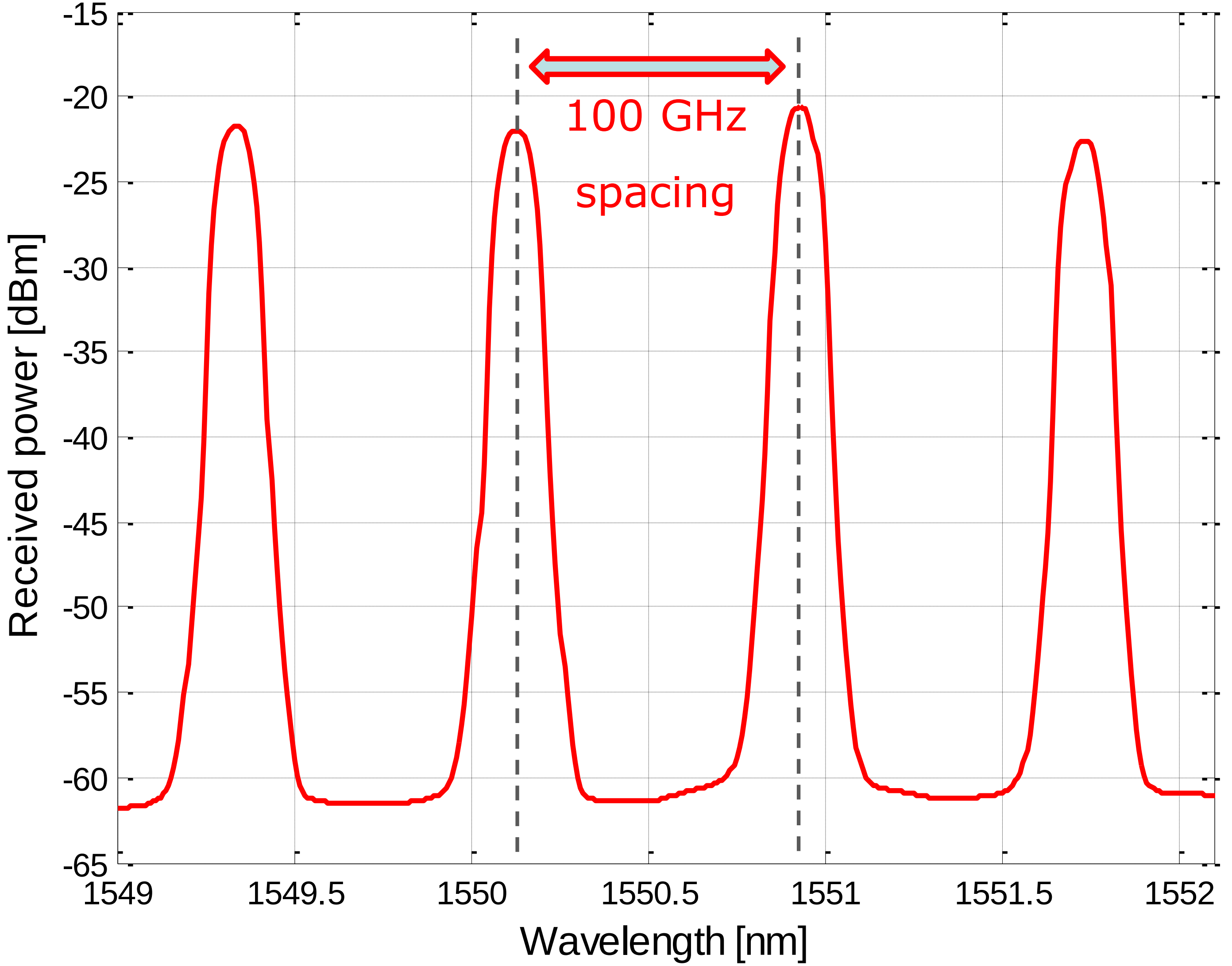
4λ WDM setup, NET bitrate per ONU= 1Gbps



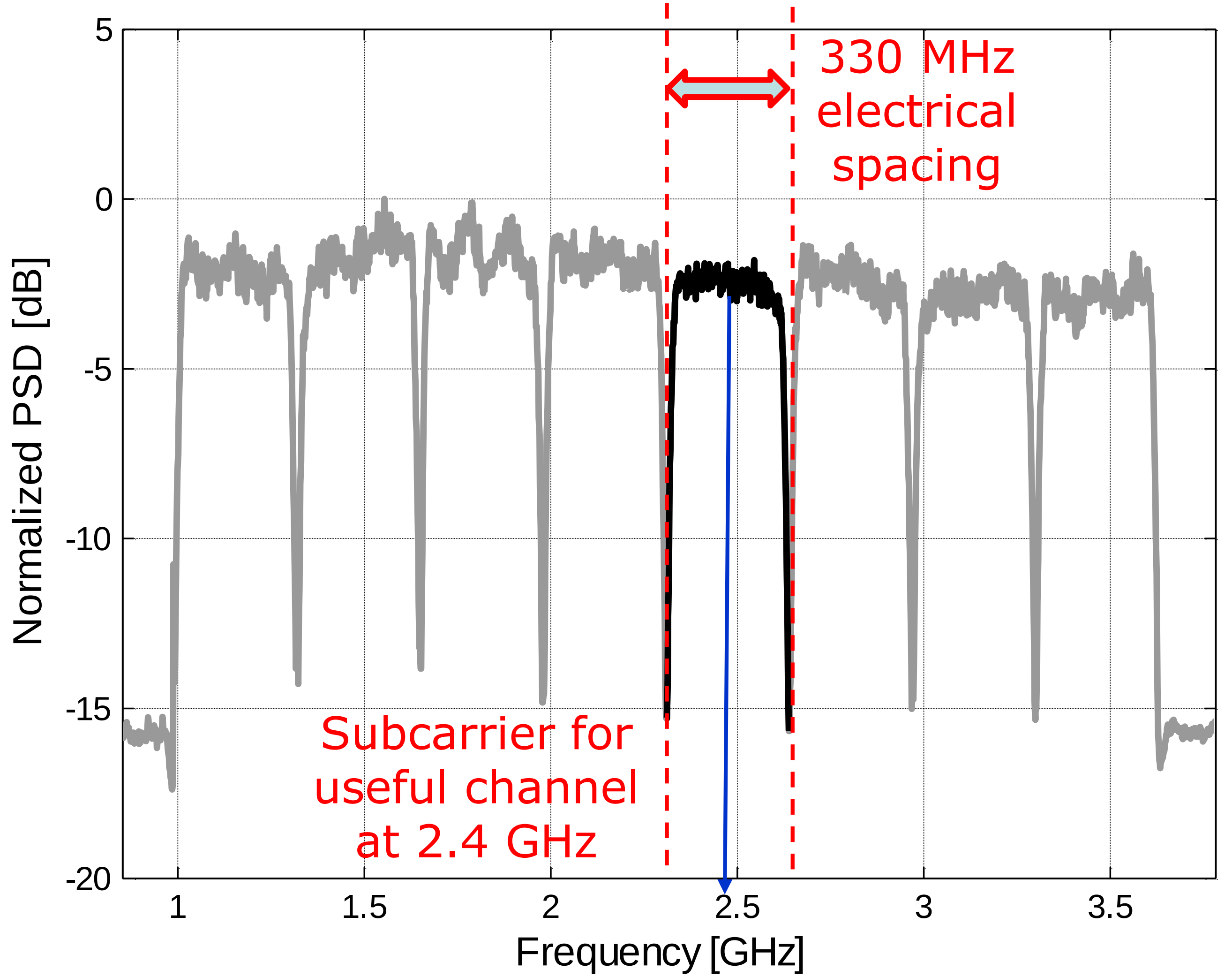
Upstream WDM setup



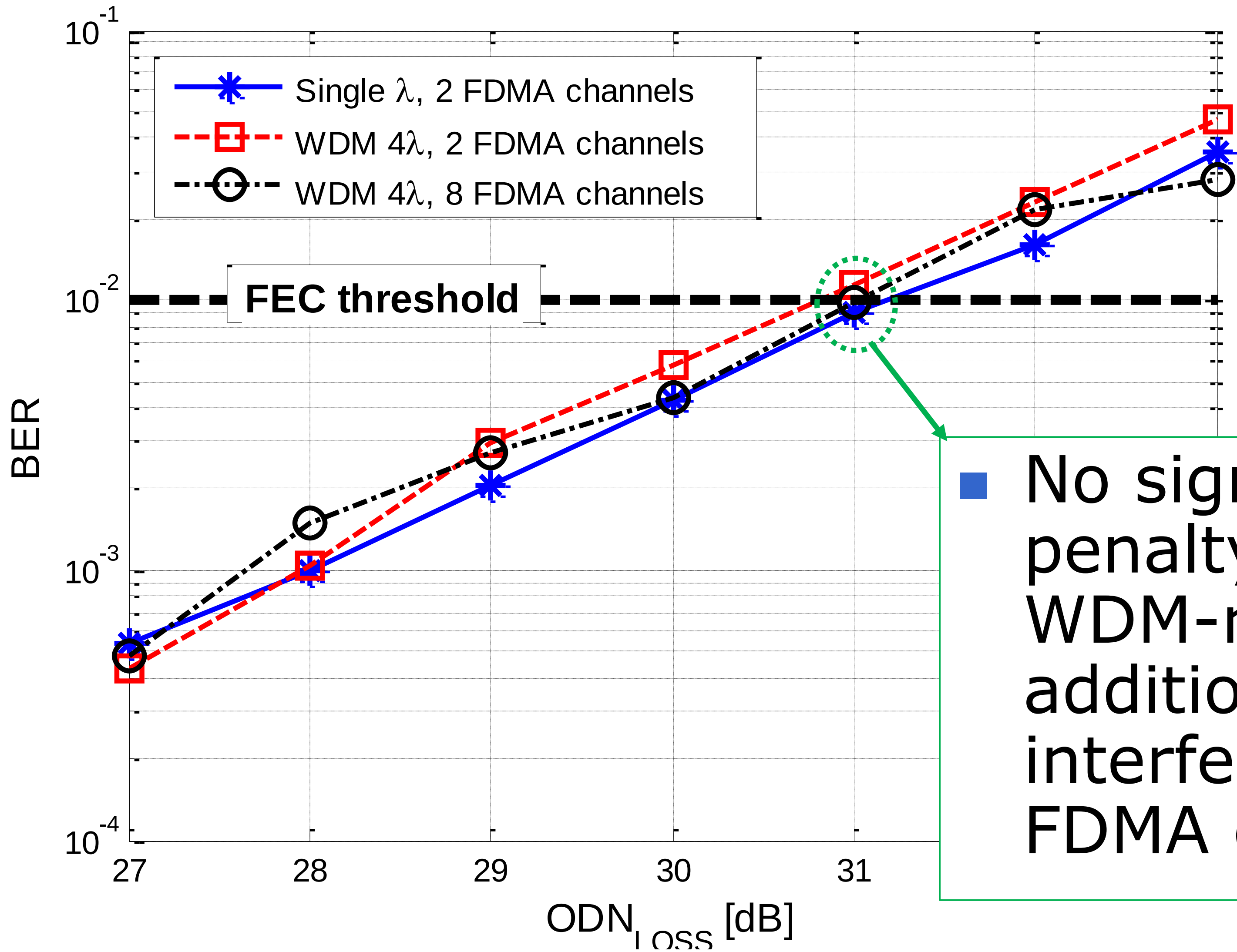
Wavelength allocation



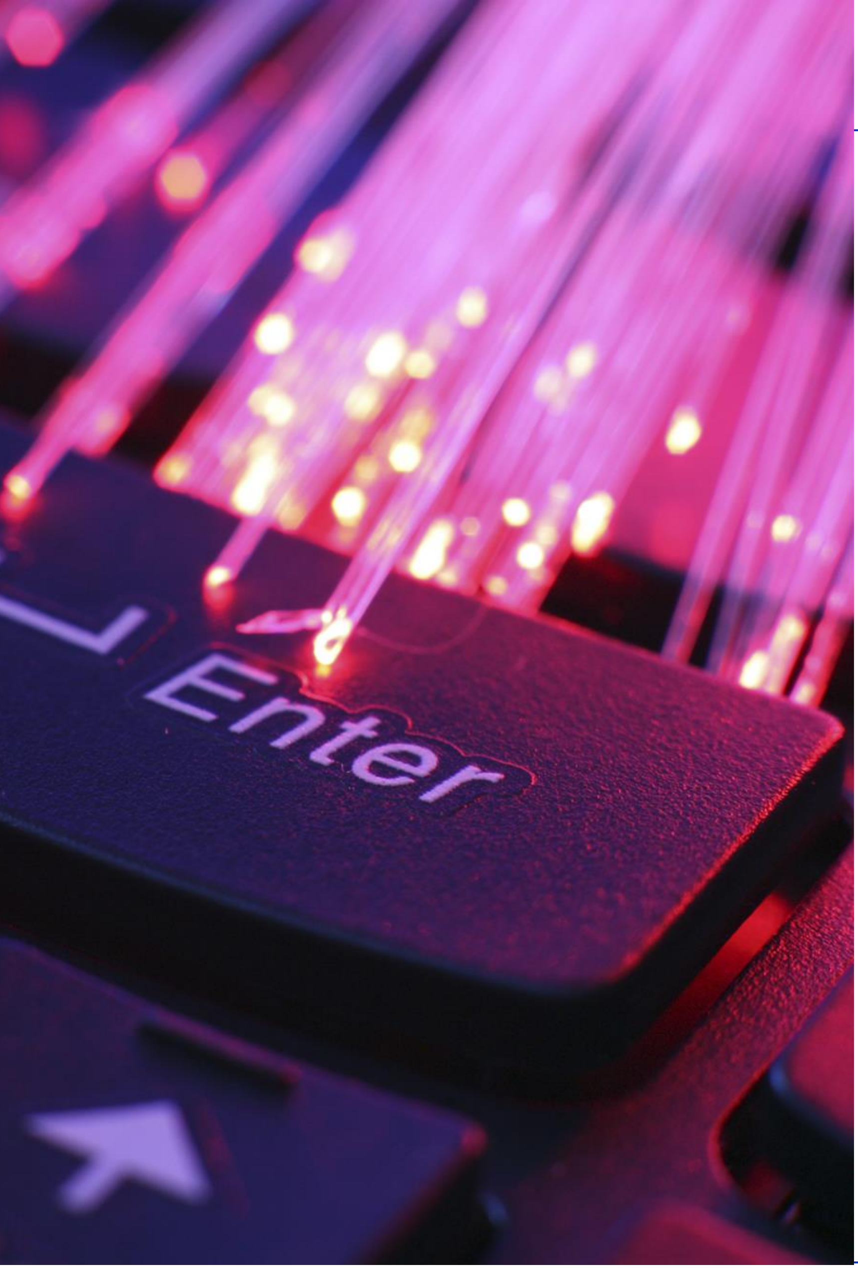
Electrical spectrum



Upstream WDM setup, NET bitrate = 1Gbps



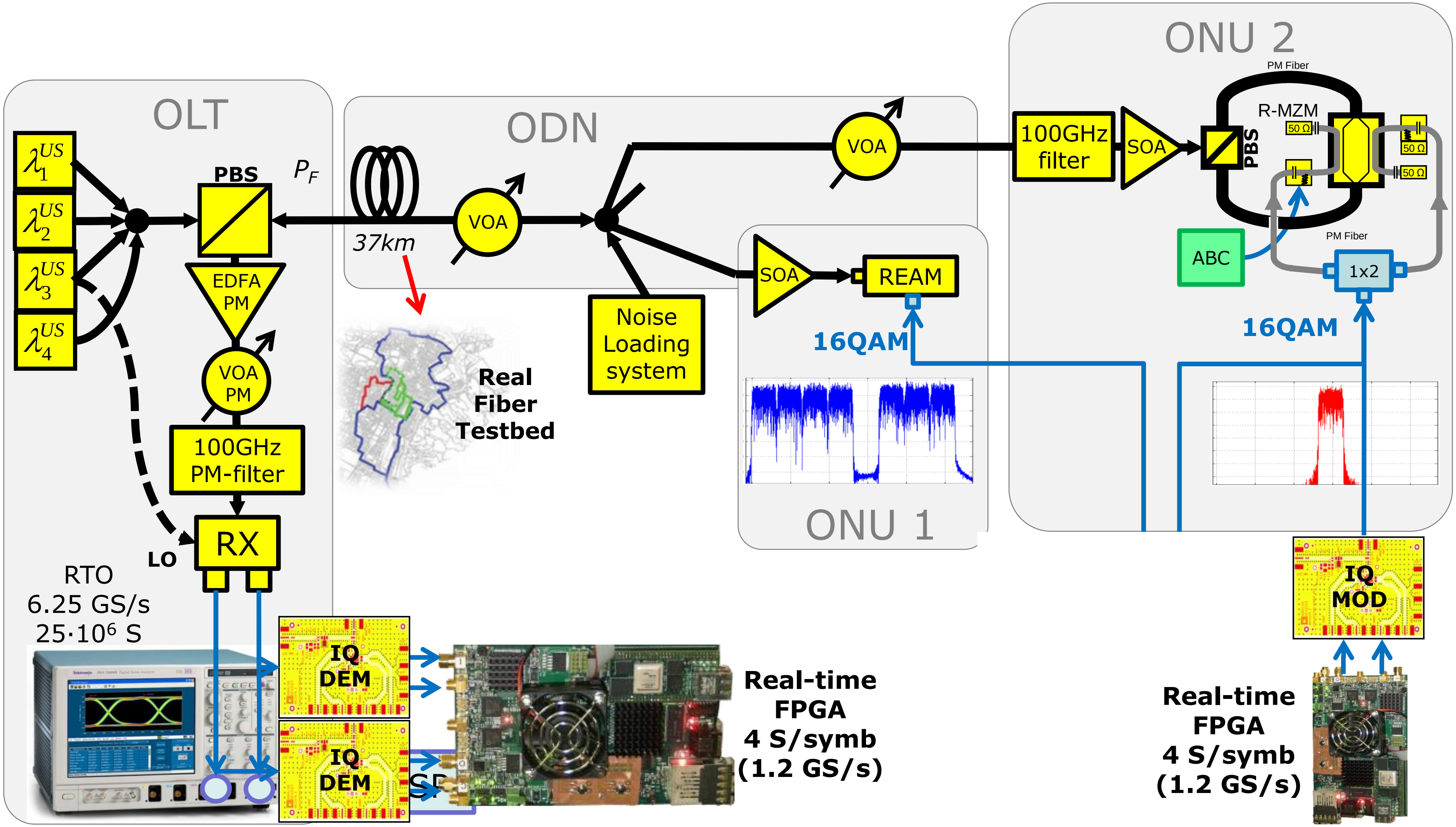
- No significant penalty due to WDM-related additional interference on FDMA channels



Real time FPGA Implementation and Experiments

(on upstream)

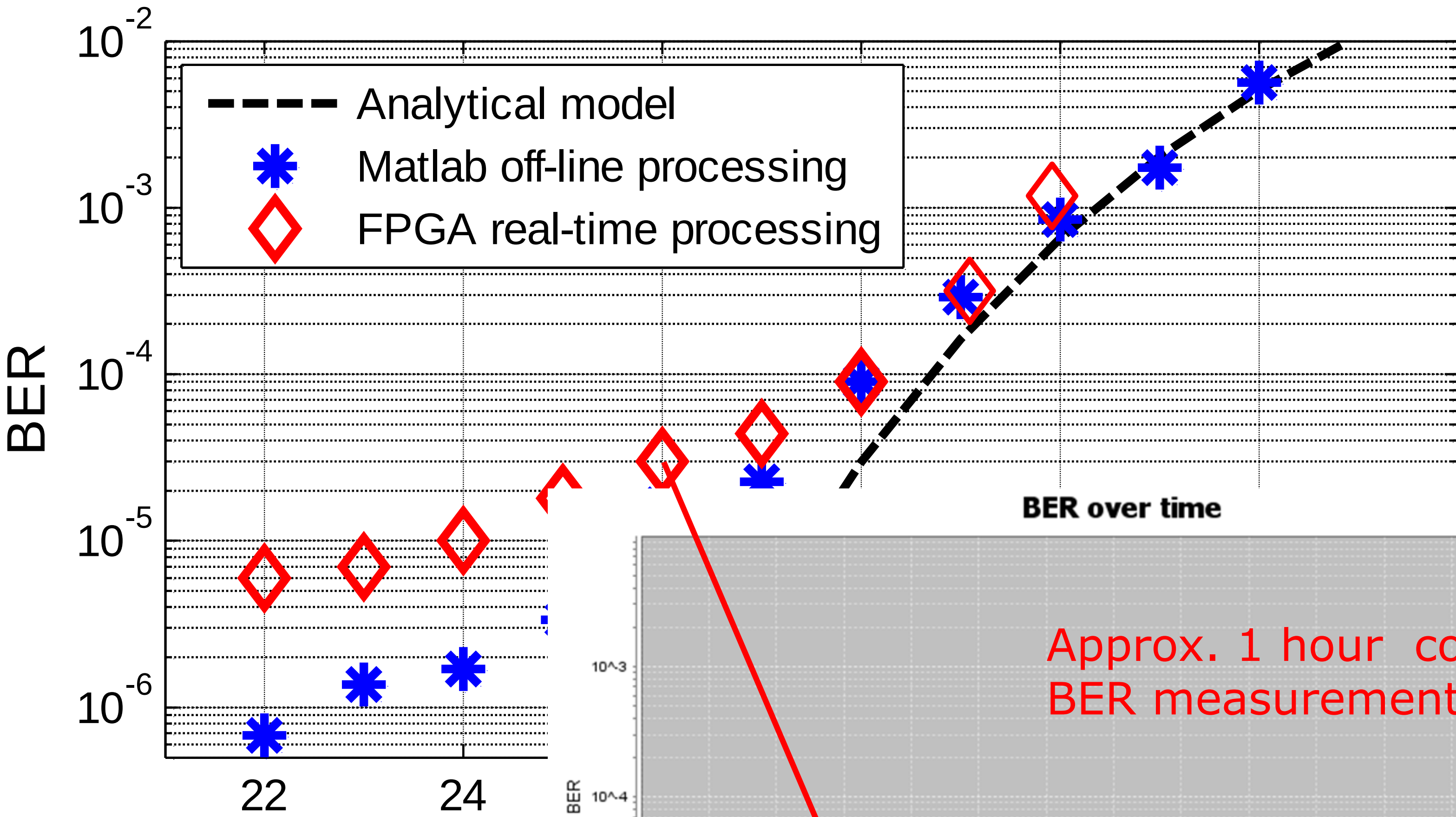
Upstream WDM setup, NET bitrate = 1Gbps

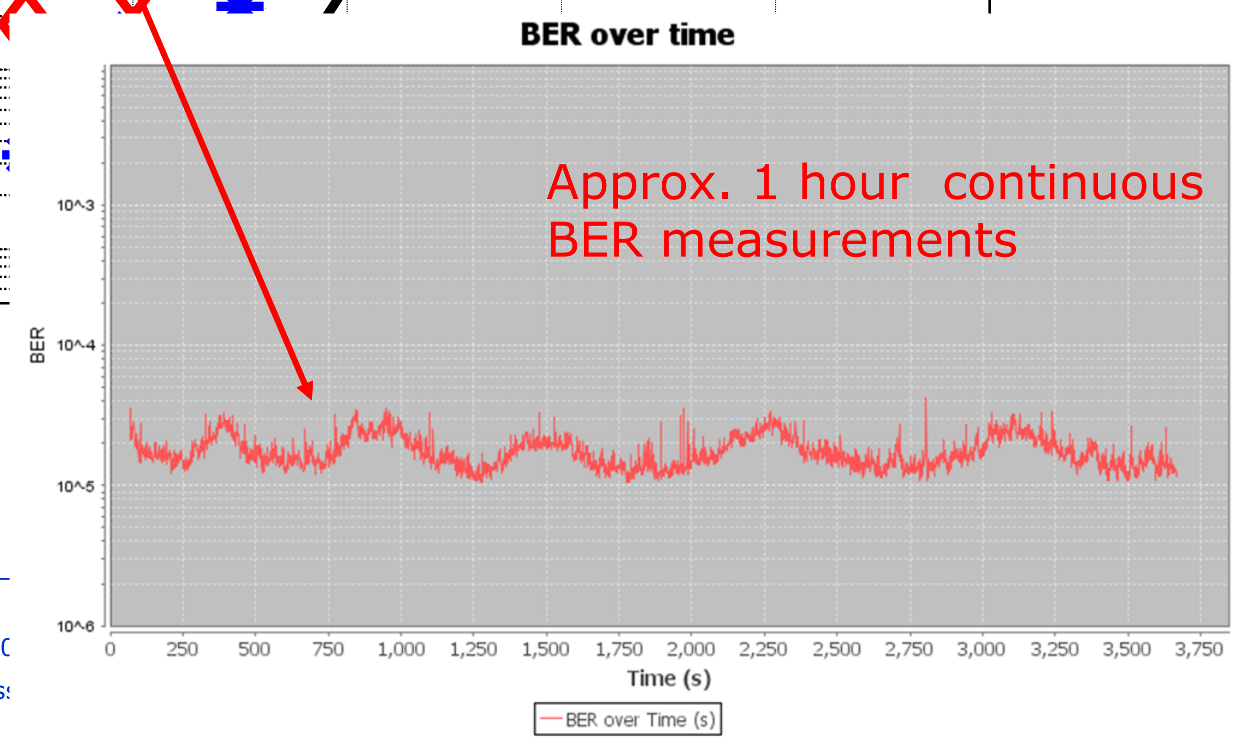


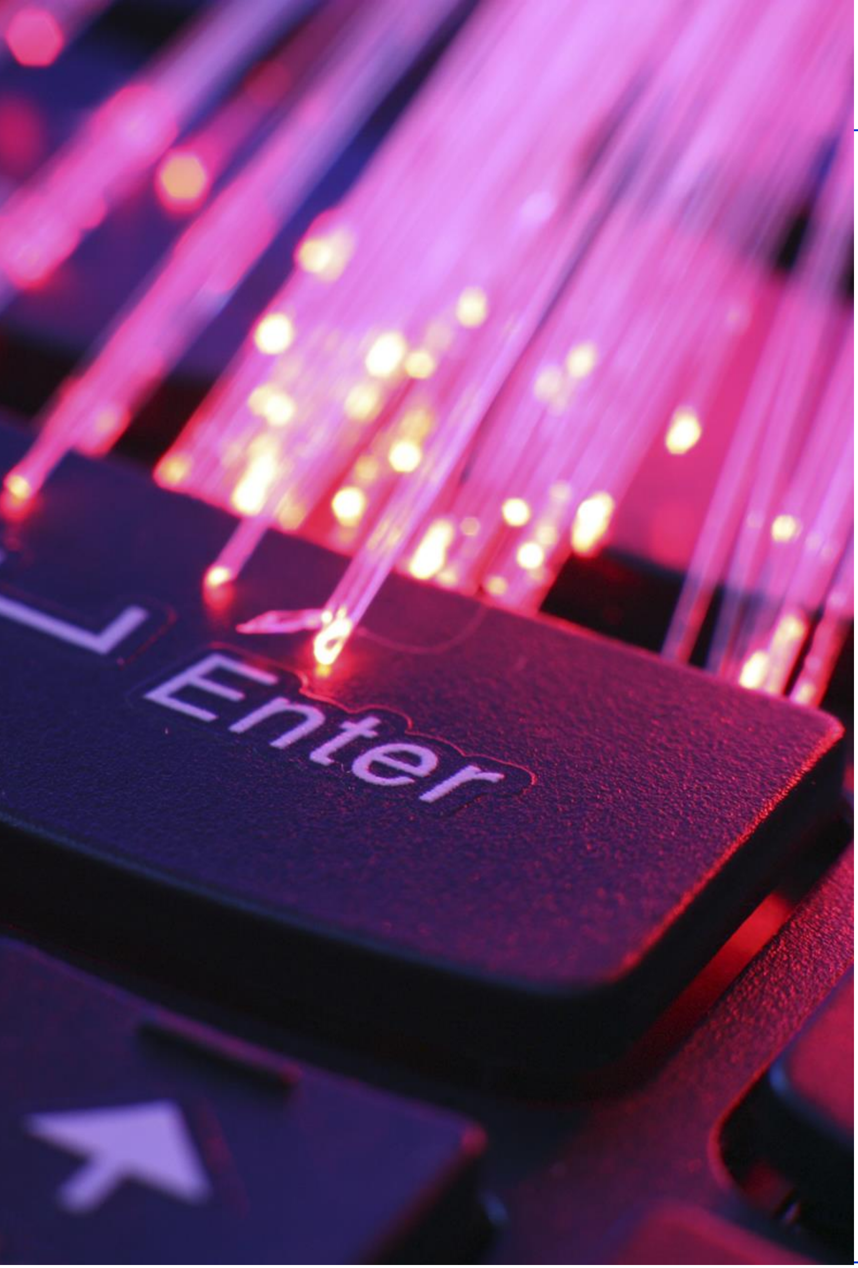
FPGA details

- The <u>ONU real time transmitter </u>is built around a Bitsim UHAB board, based <u>on two Virtex4-SX35 FPGAs</u>, two 1.2 GS/s DAC converters and a dual channel 1.2 GS/s ADC
- The <u>OLT RX real time DSP </u>demonstrator is built around a Xilinx VC707 board equipped with a <u>Virtex7 XC7VX485T FPGA</u>, connected to a Texas Instruments ADC that samples two electrical channels at 1.2 GS/s.

Upstream WDM setup, NET bitrate = 1Gbps





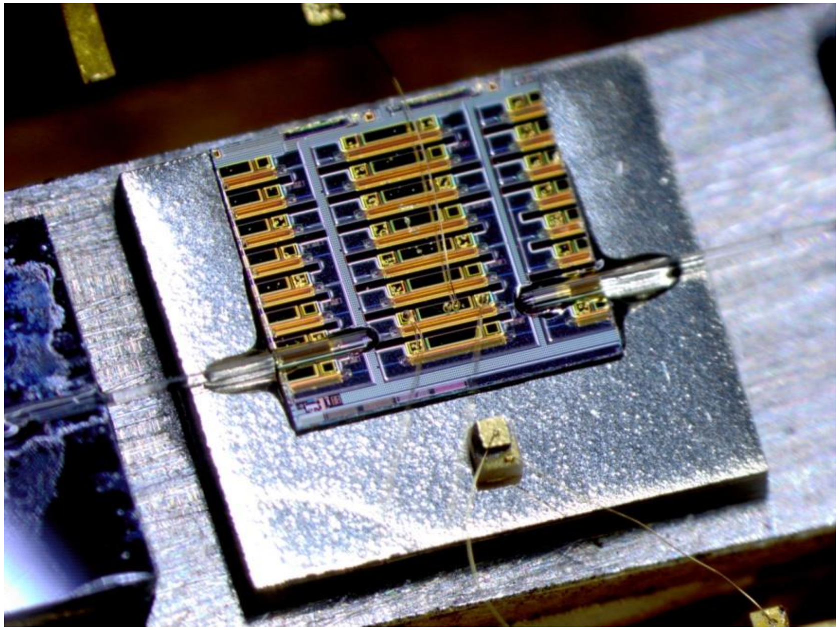


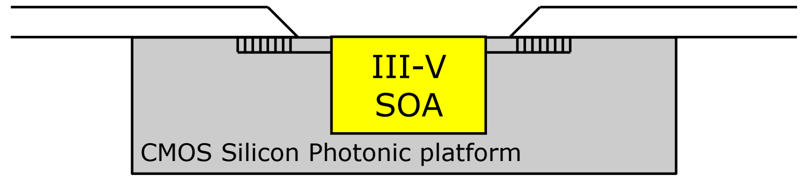
Future work & Conclusions

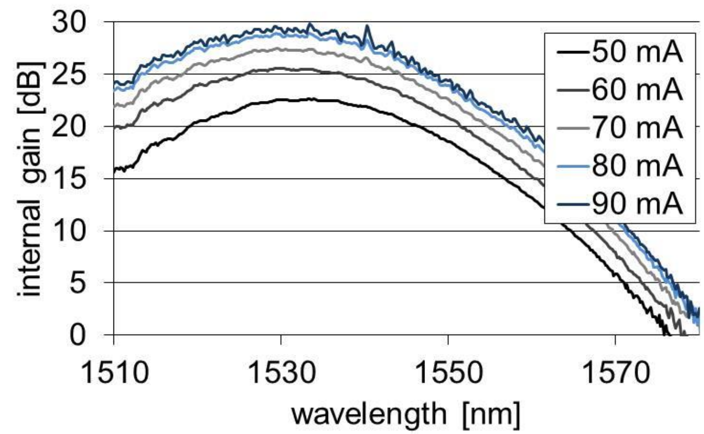
The project workpackage on components

- Silicon Photonic integration is a key enabling factor toward a feasible techno-economic for this solution.
  - Will the integrated components guarantee the same performances we obtained using discrete (and expensive) optoelectronic components?

Packaged Hybrid III-V/silicon SOA







INTERNAL GAIN

- Up to 28±2 dB internal gain
  - λ-shift between fiber-to-fiber and internal gain due to grating coupler characteristics

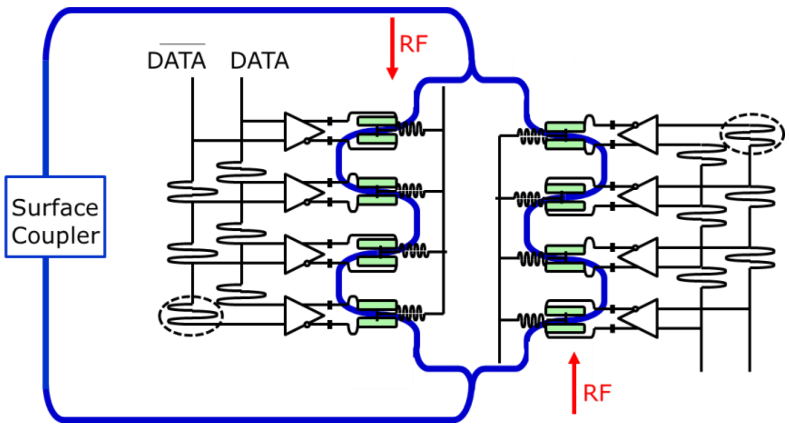
[3] P. Kaspar et al., "Packaged Hybrid III-V/Silicon SOA", ECOC 2014, Cannes, France

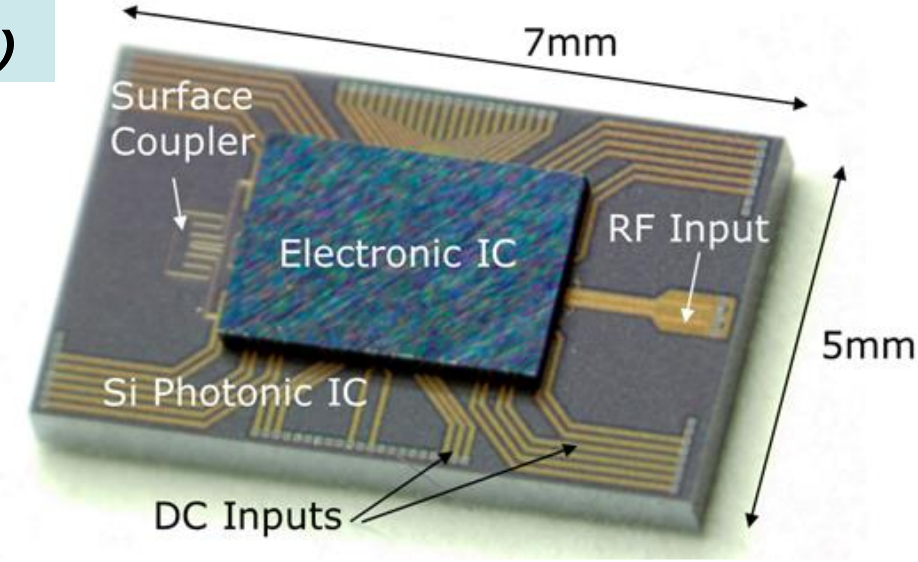
R-MZ Modulator and Driver integration

Distributed driving architecture

Photonic IC = Silicon Photonics ***(CEA)***

Elec IC = BiCMOS ***(ST Microelectronics)***

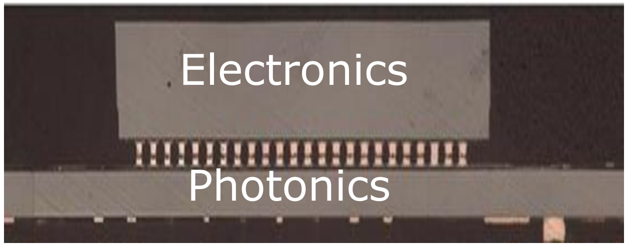




3D integration of Photonic & Electronic ICs

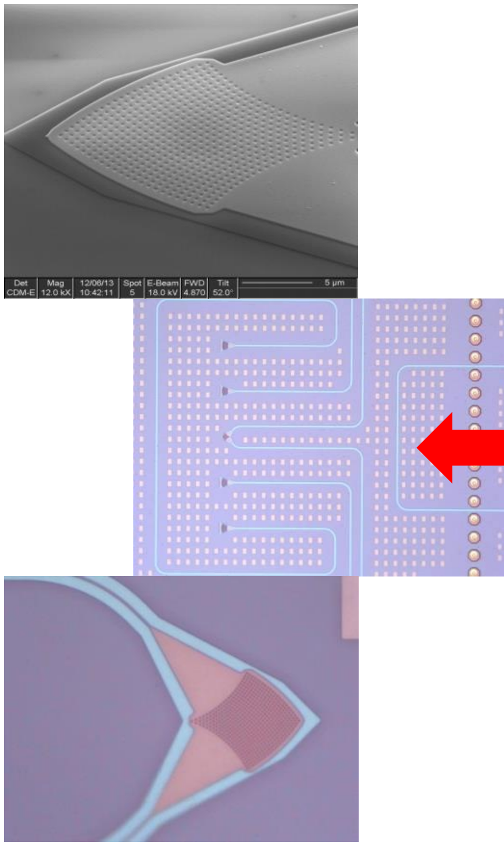
Micro bumps from 3D standard process (CEA)

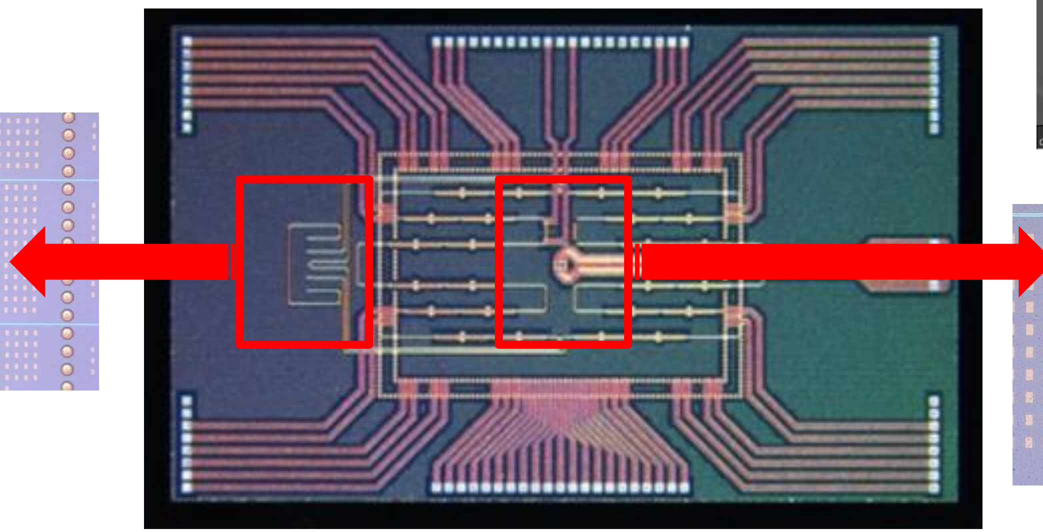
- ➔ *reduced parasitic capacitance*
- ➔ *Dense interconnections (40µm-pitch)*

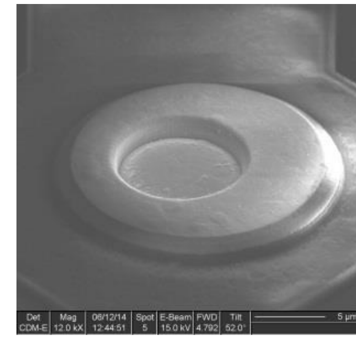


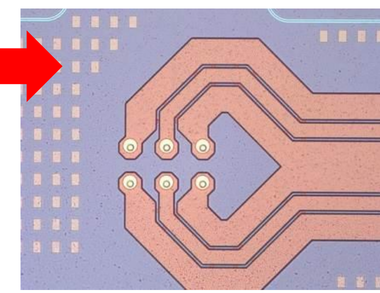
Photonic Integrated Circuit Manufacturing

SOI 220nm/2000nm Oxide technology
Processed at Leti on 200mm wafer









RF electrodes with pads for bump interconnections

Optical Coupling structures

Conclusions

- We have demonstrated an FDMA Self-coherent R-PON delivering 4x32 Gbps in the upstream direction
  - Up to ODN loss of 31 dB (ITU-T class N2) and DOPL of 15 dB.

- The proposed setup may allow great flexibility in allocating bit rate to different types of users (using approaches similar to OFDM bit loading)
  - This feature may enable coexistence of super-users, such as mobile operators, with residential users on the same PON

Thanks for your attention!

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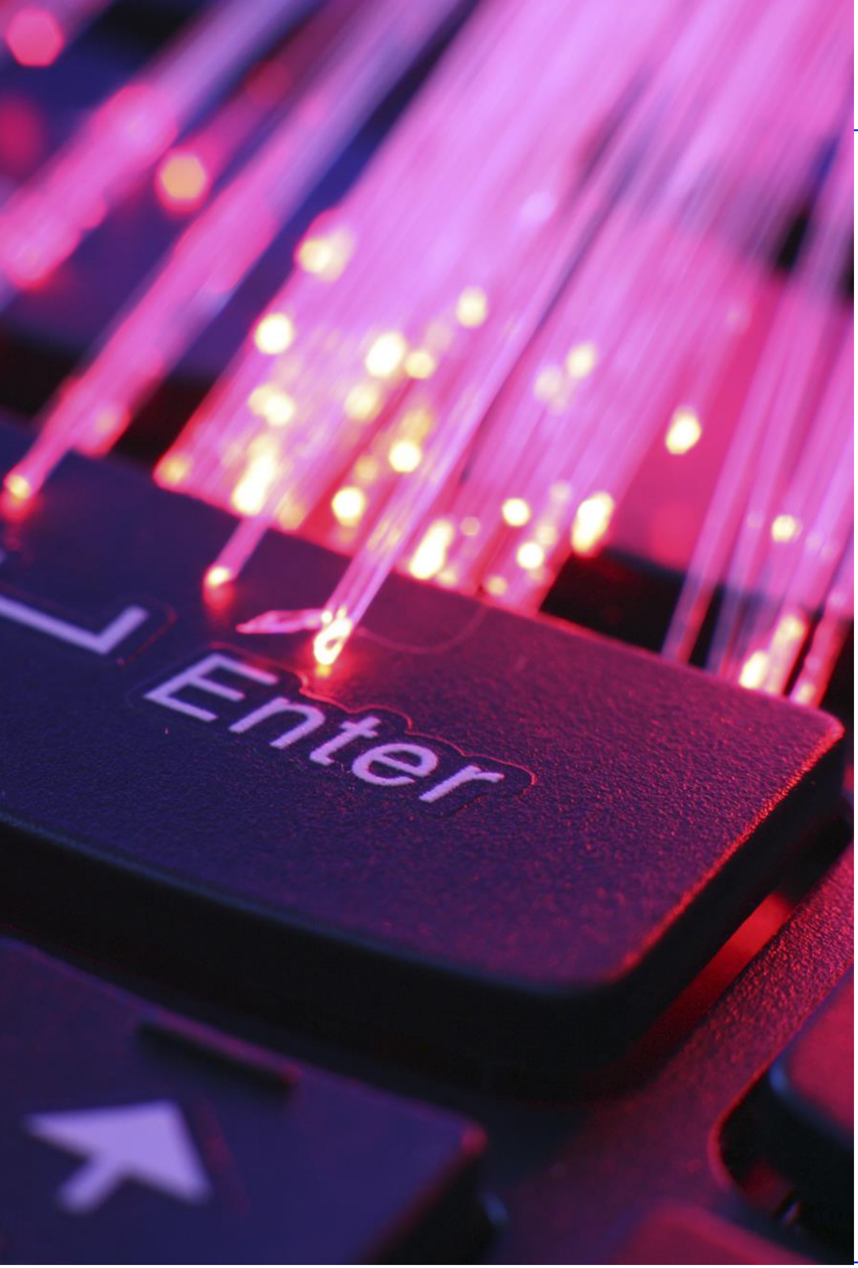

Backup slides

The OLT

Faraday rotation at ONU allows symplified single polarization coherent detection at the OLT