Real Time implementation of upstream FDMA-PON over an FPGA platform: Results from the UE project FABULOUS

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FP7-ICT-2011-8 Challenge 3.5 – STREP project n. 318704 – FABULOUS
FDMA Access By Using Low-cost Optical Network Units in Silicon photonics

The ideas behind Fabulous

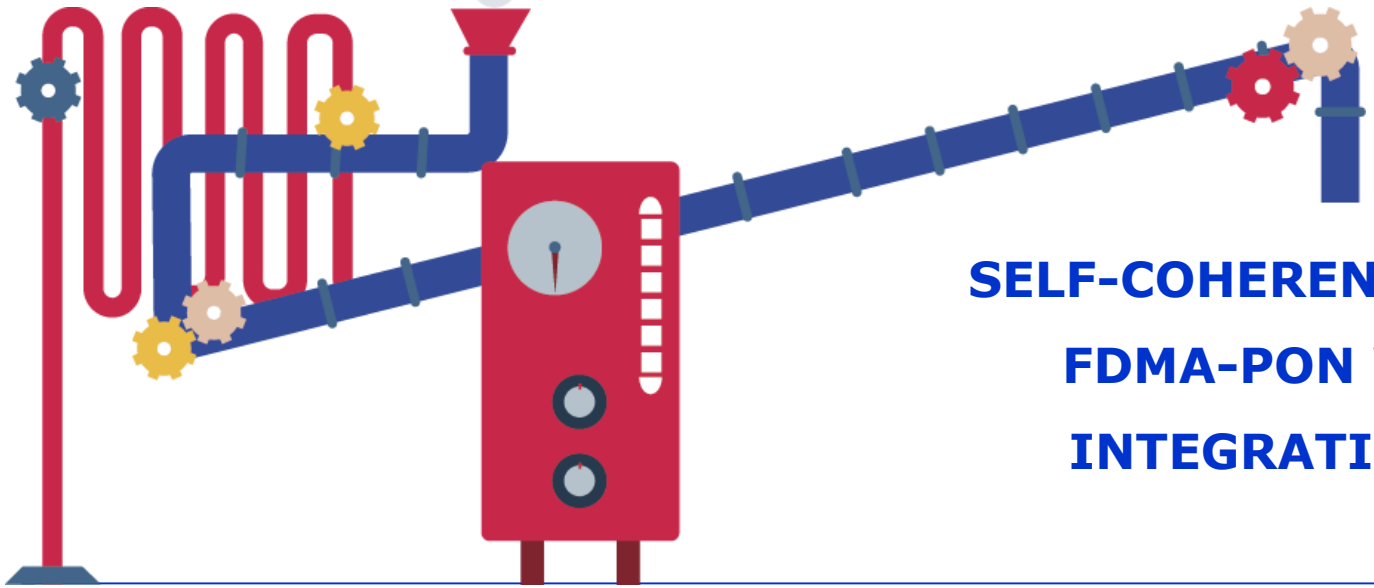
Flexible network

High capacity

ITU-T ODN compliant

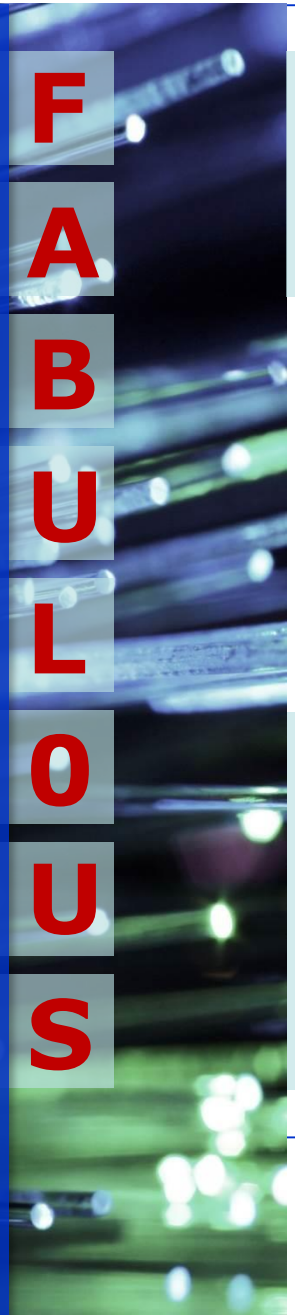
No uncontrolled λ at ONU switch-on

High level of optical integration



SELF-COHERENT REFLECTIVE FDMA-PON WITH ONU INTEGRATION ON SiP

FABULOUS at-a-glance



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ARCHITECTURE

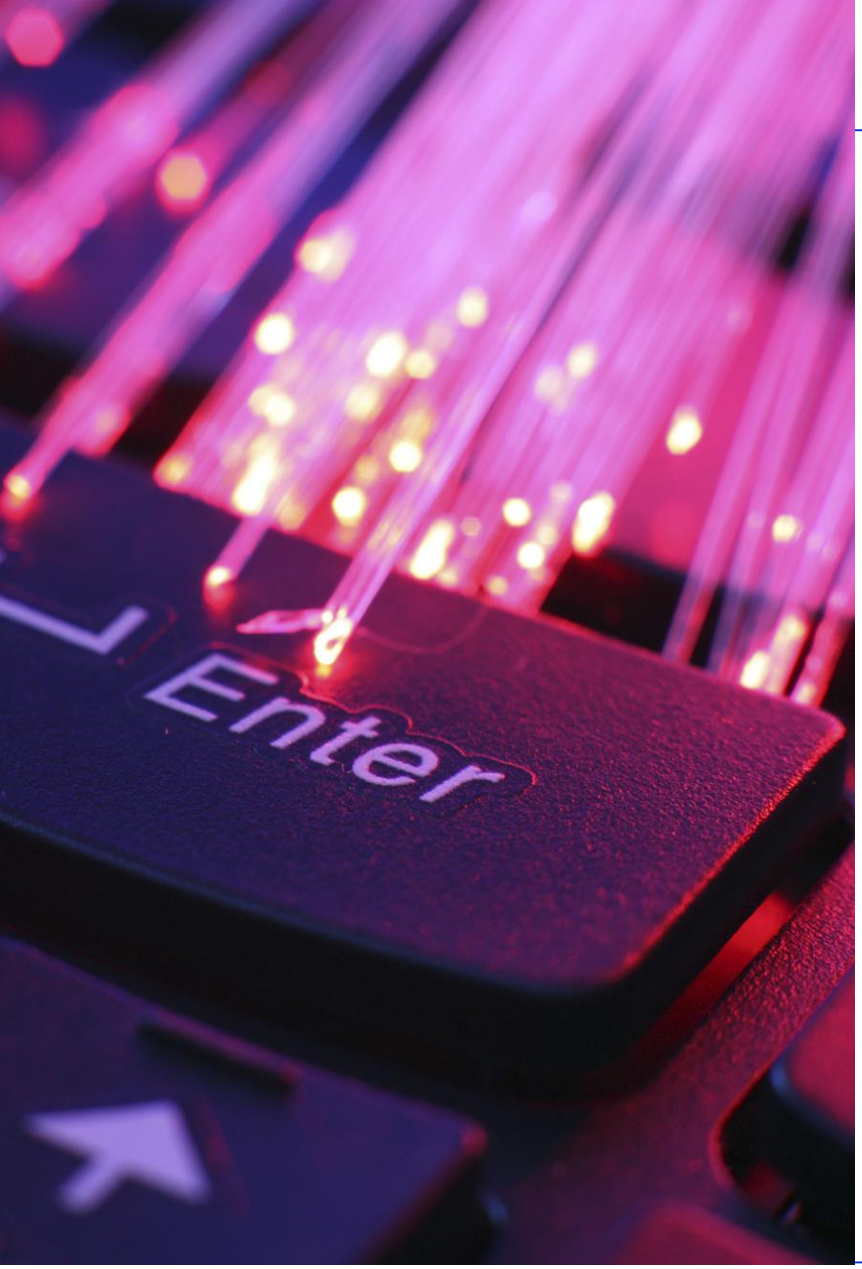
SYSTEM PARAMETERS

FP7-ICT-2011-8 – Objective 3.5: Core and disruptive photonic technologies

"Application-specific photonic components and subsystems"

"For access networks, the goal is affordable technology enabling 1-10 Gb/s data-rate per client"

NEW COMPONENTS

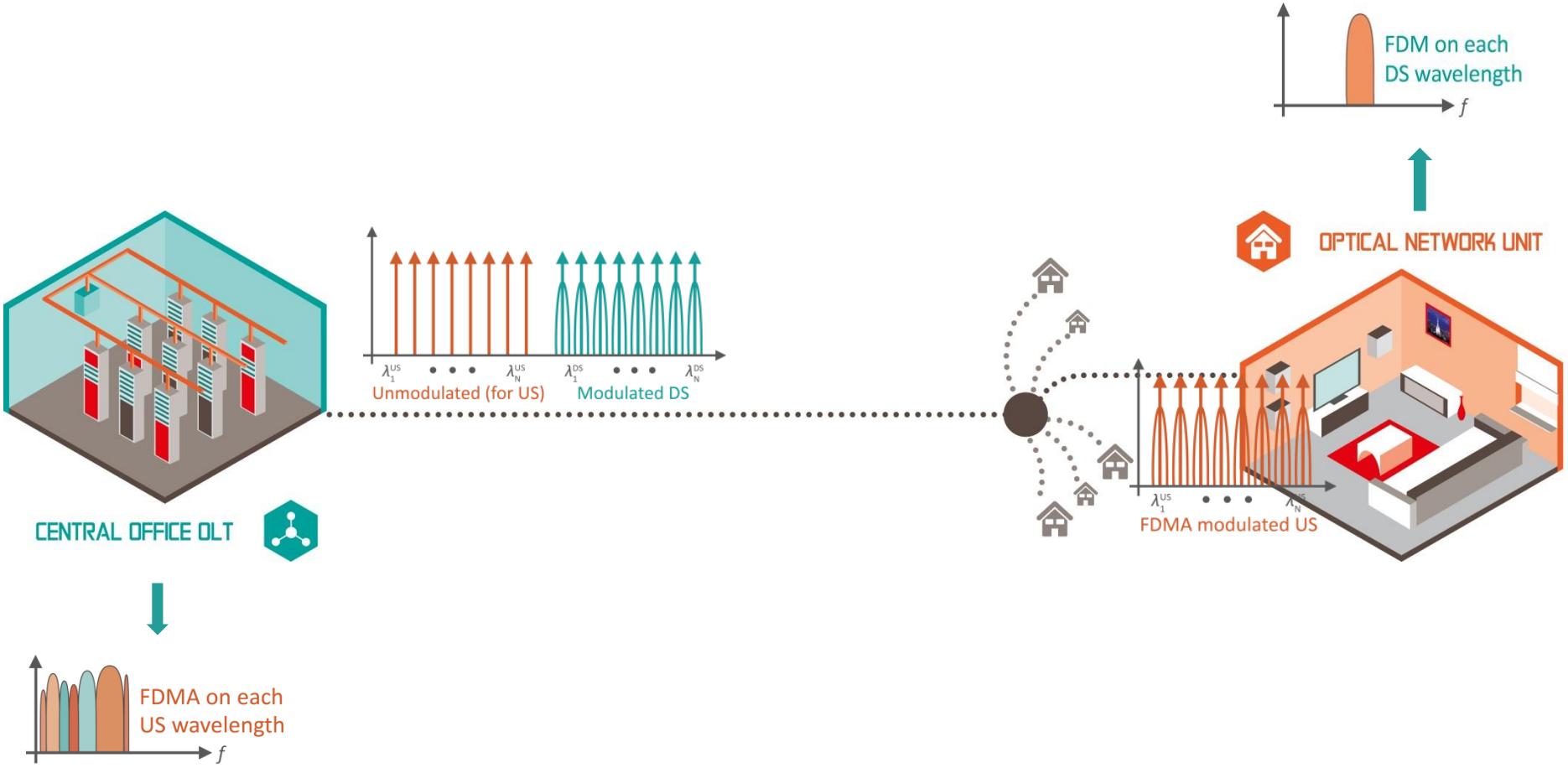


SUMMARY

- **Concept description: architecture and components**
- **Experimental setup**
- **DSP FPGA implementation**
- **Conclusions**

The general architecture

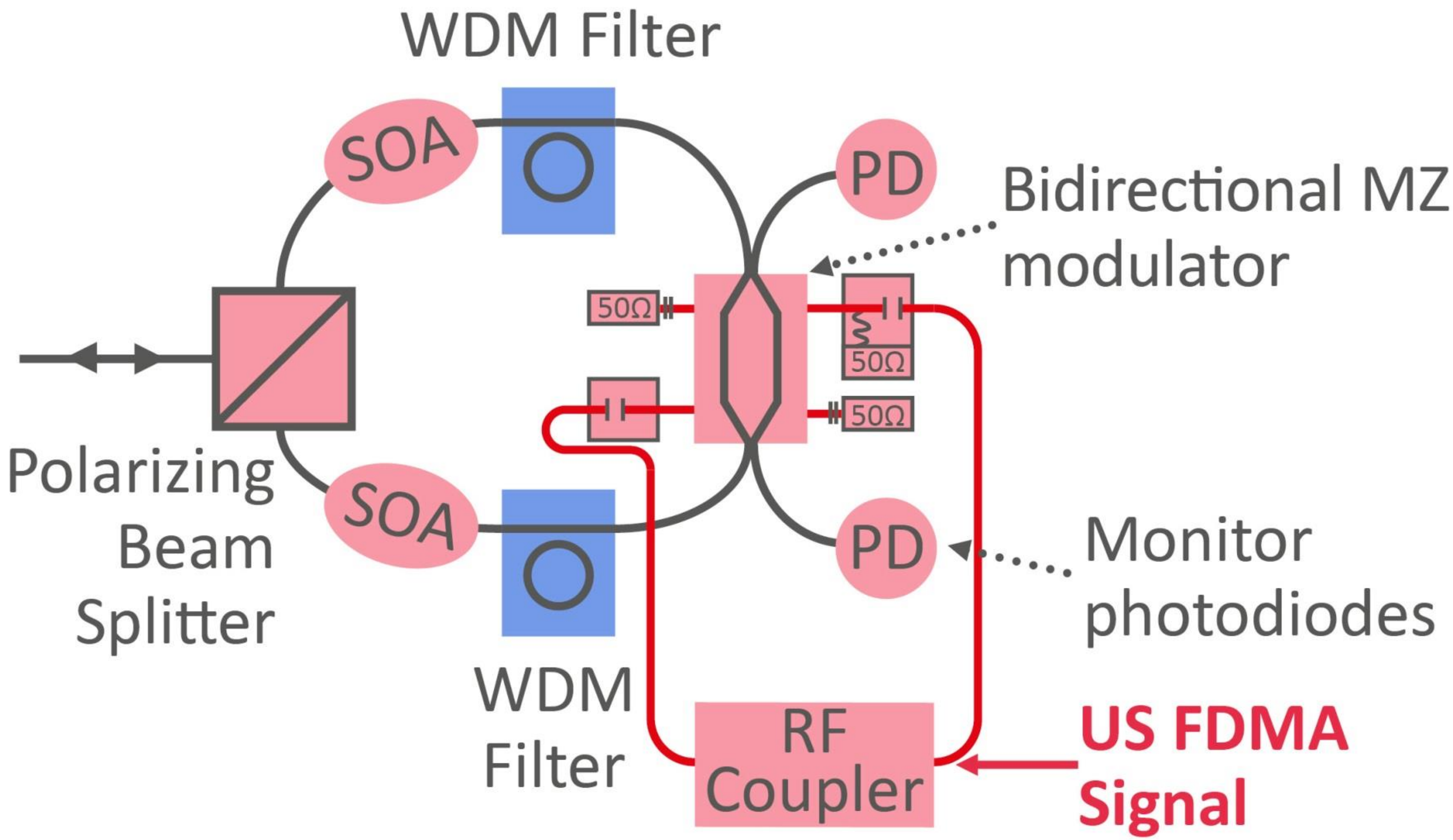
Reflective WDM PON based on FDM / FDMA



The ONU

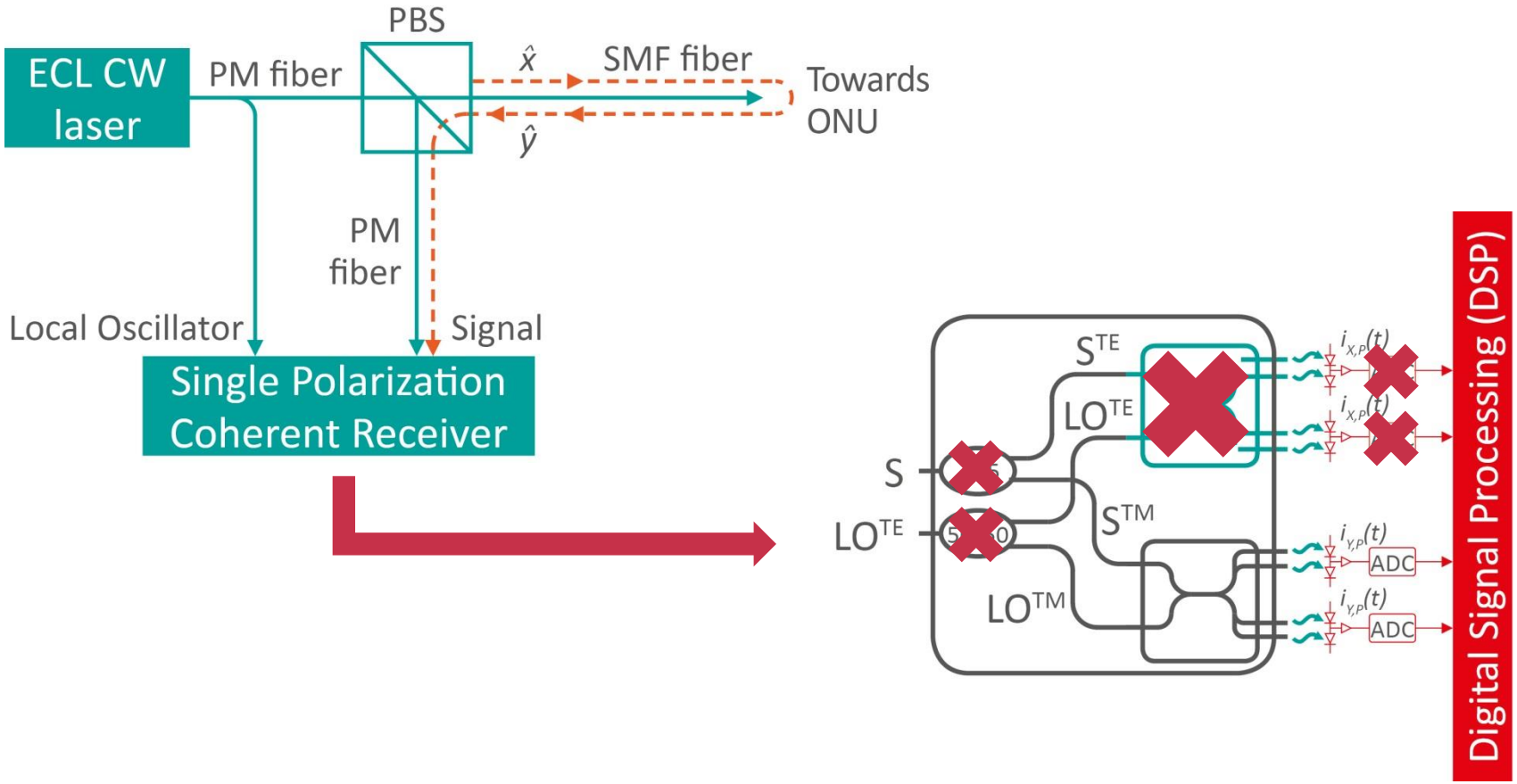
The ONU reflects the seed signal, modulates it and performs 90° polarization rotation

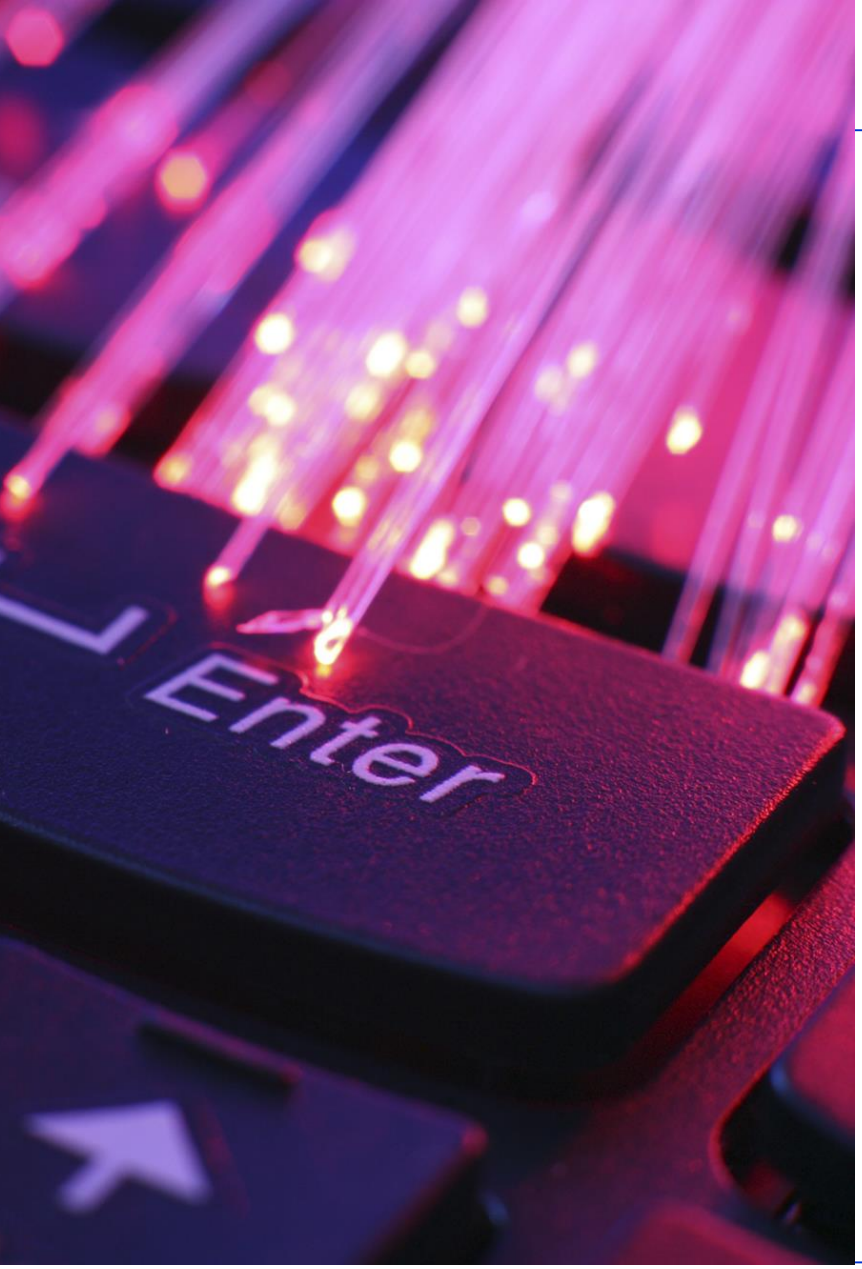
Purpose of the project is to integrate the ONU on a Silicon Photonic PIC



The OLT

Polarization rotation allows symplified coherent detection at the OLT





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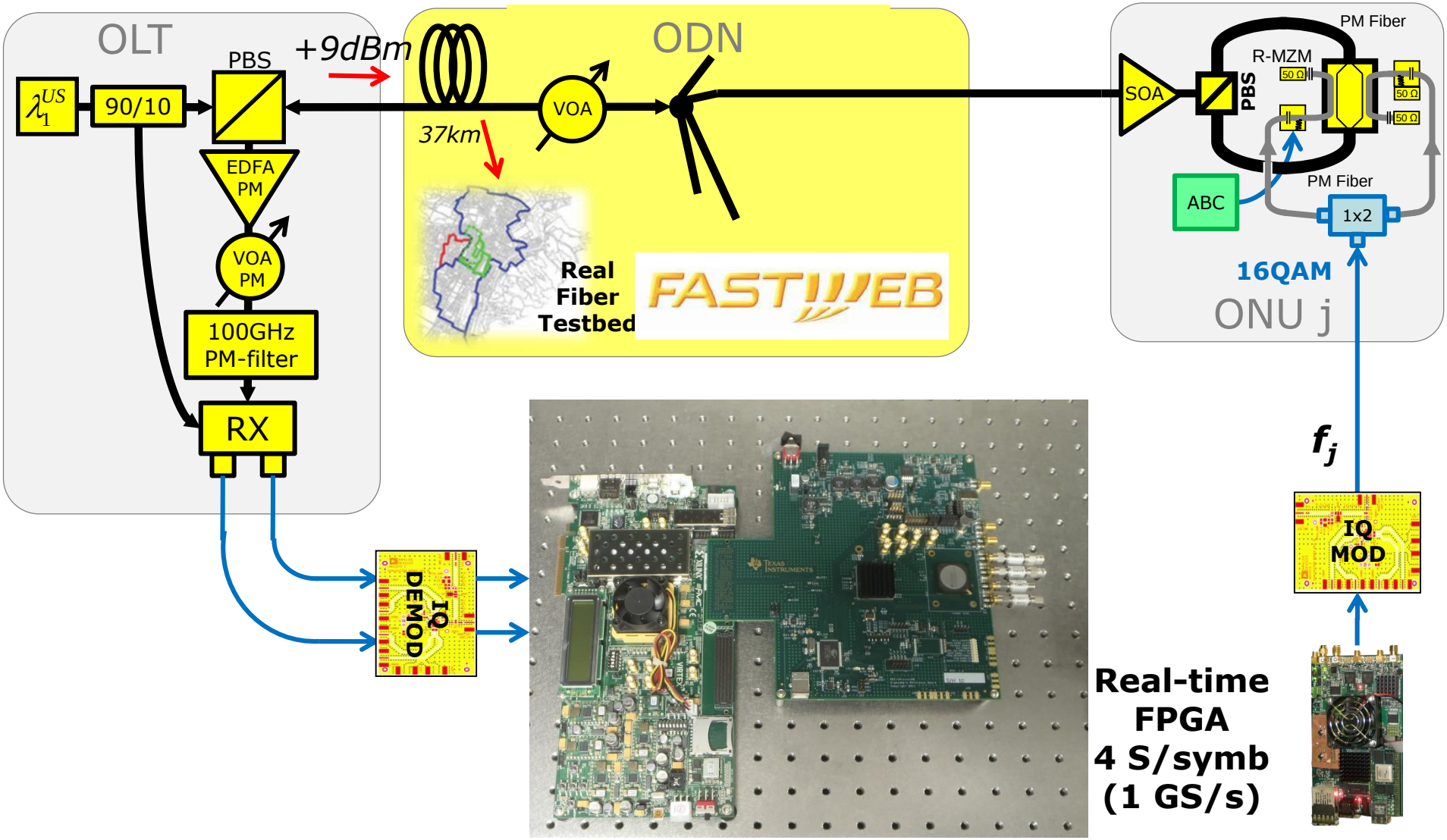
Upstream setup



Setup for this set of experiments

DATA RATE PER USER SET AT 1 GBPS

- (net data rate, giving a gross rate of 1.2 Gbps including FEC, overhead and line coding)

MODULATION FORMAT SET AT 16-QAM

- Raised cosine spectrum, roll-off=0.1
- Requires B~330 MHz per user

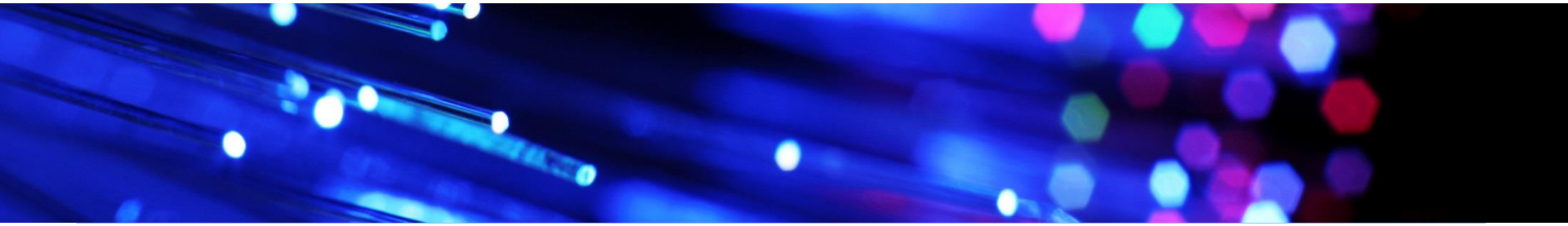
FDMA Channel selection

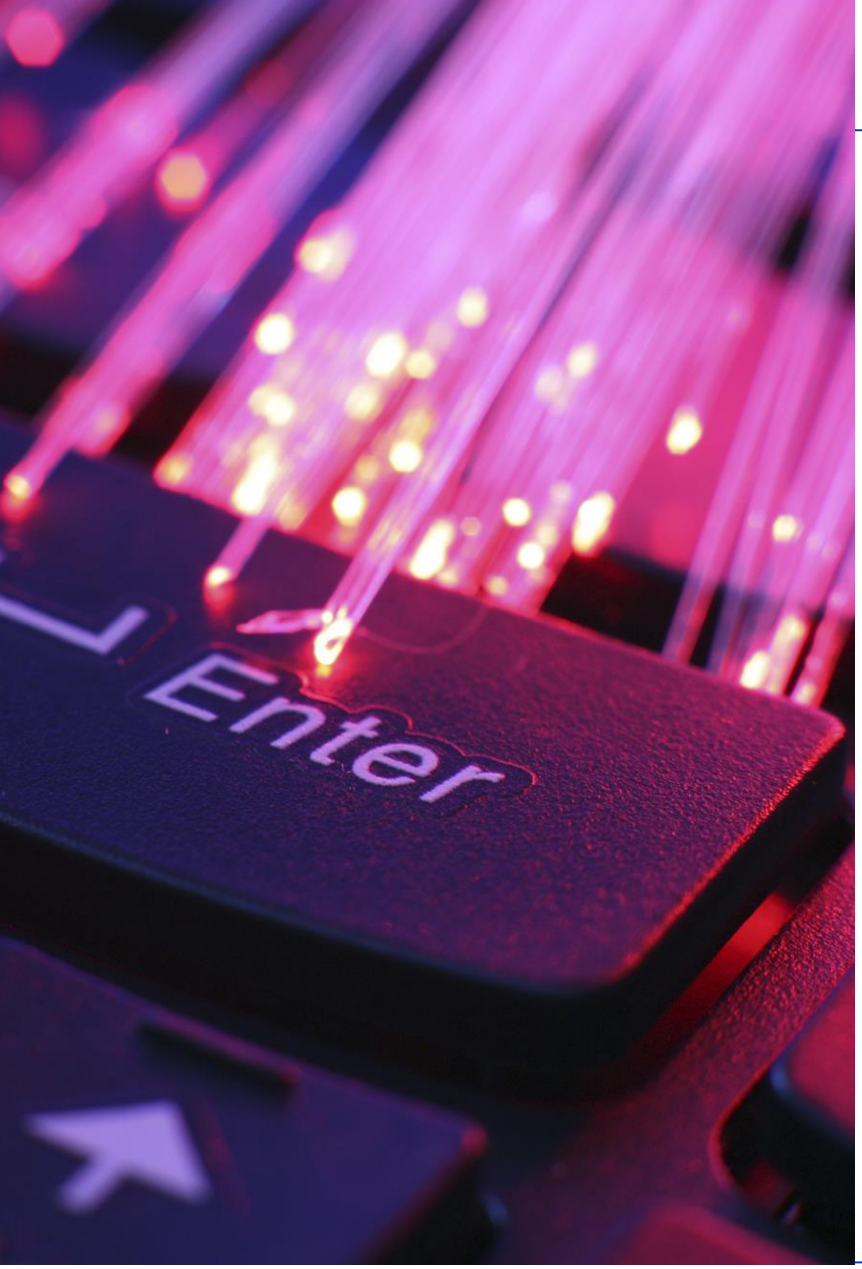
- 2 GHz Local oscillator for IQ modulator and demodulator

Digital signal processing: starting point

- Off-line processing experiments. Sampling at 12,5 GS/s with RTO and down-conversion
- Development of DSP algorithms suitable for the FPGA implementation
  - Running at ~600MS/s – sub-band processing
  - Feed-forward adaptive equalizer with 31 complex taps updated by CMA
  - CPE using Viterbi-Viterbi

[1] B. Charbonnier, A. Lebreton, "Demonstration of Low DSP Requirements for FDMA PON", ECOC 2014, P7.4, Cannes, France





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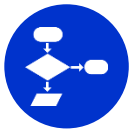
Key points when porting DSP code to FPGA

A/D and D/A now 1200 Msample/s

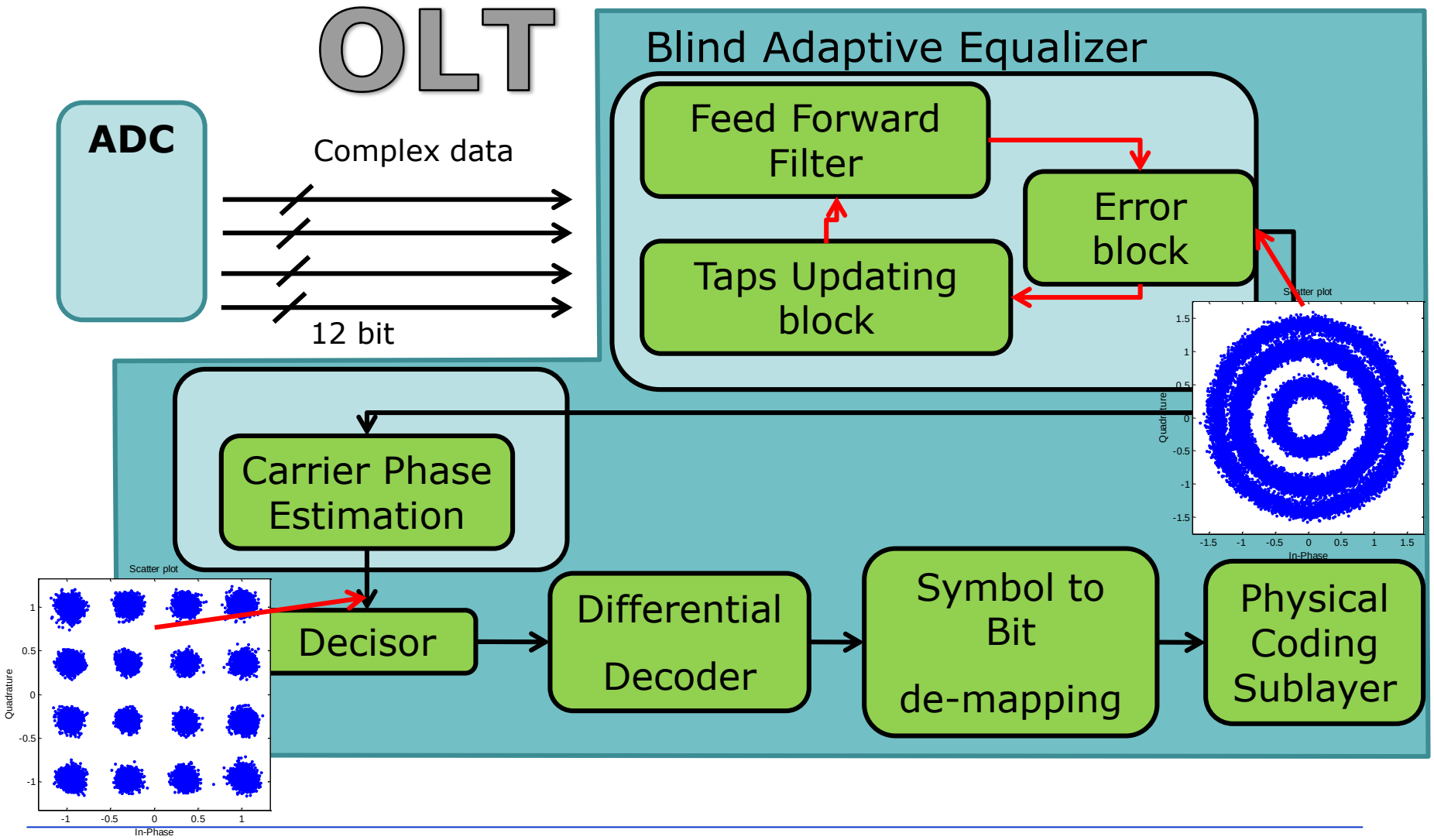
Parallel bus of 4 samples on both FPGAs



Finite math

Latency (pipeline registers)

OLT RX Main blocks and status of the design



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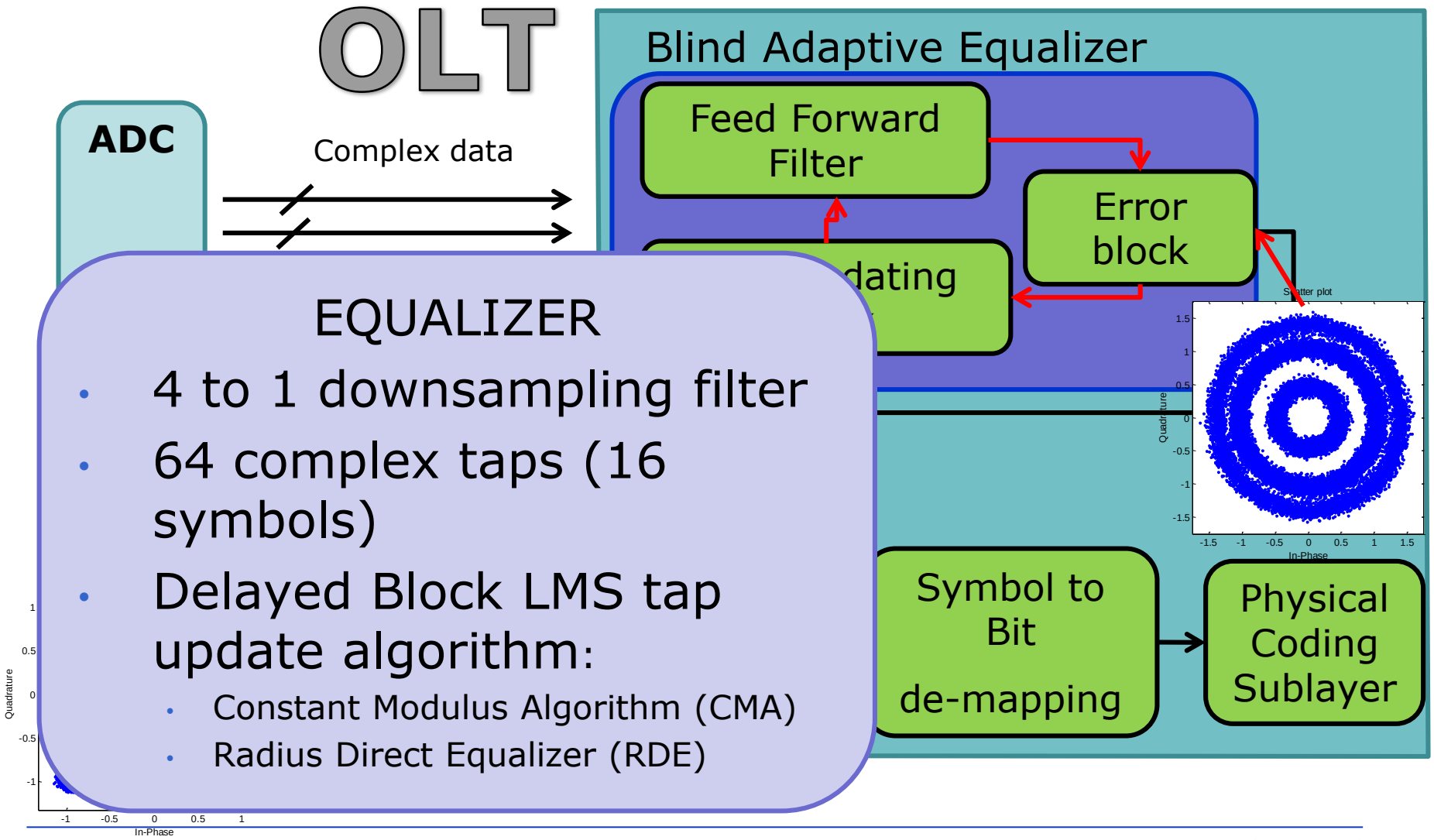

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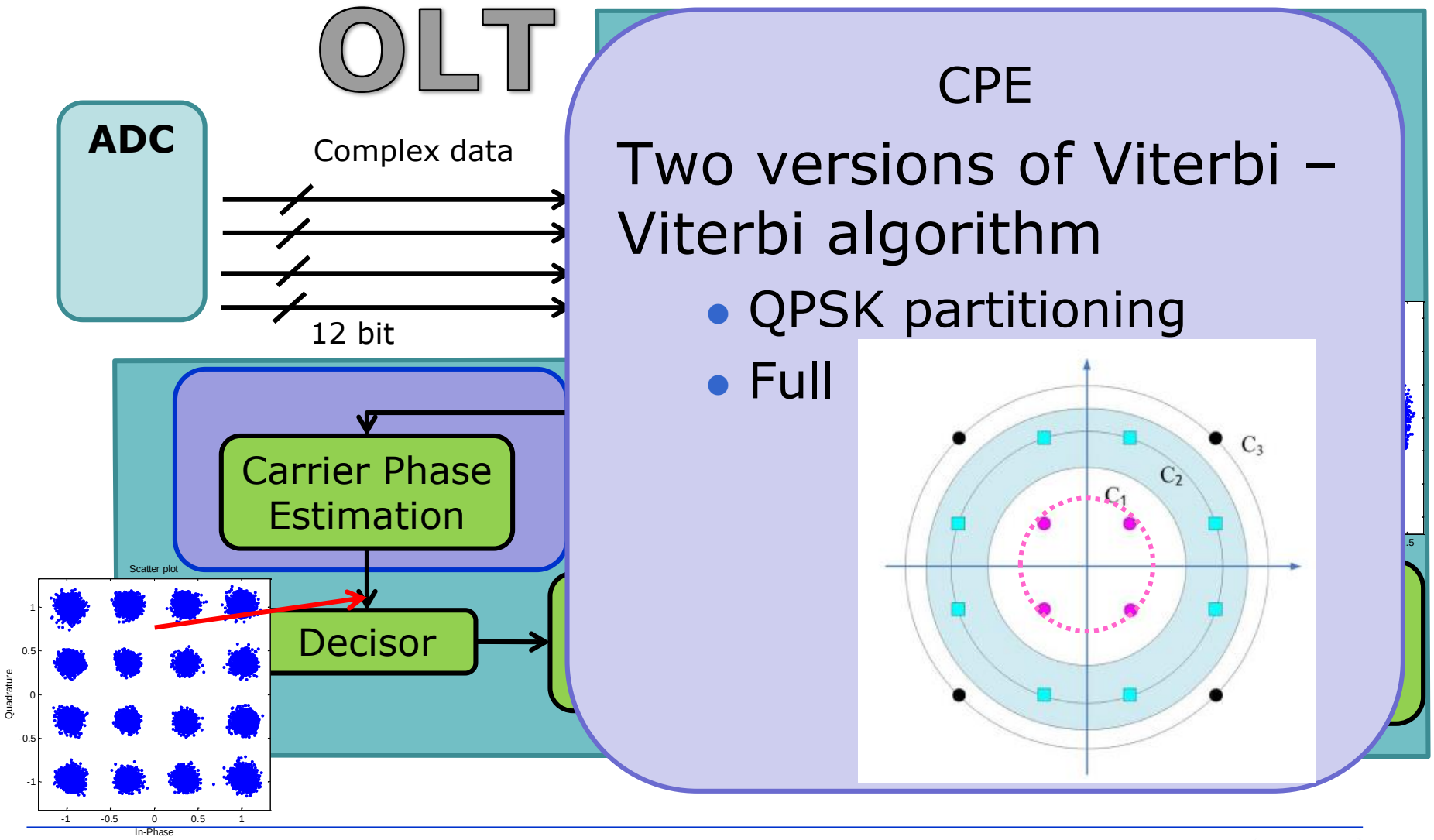

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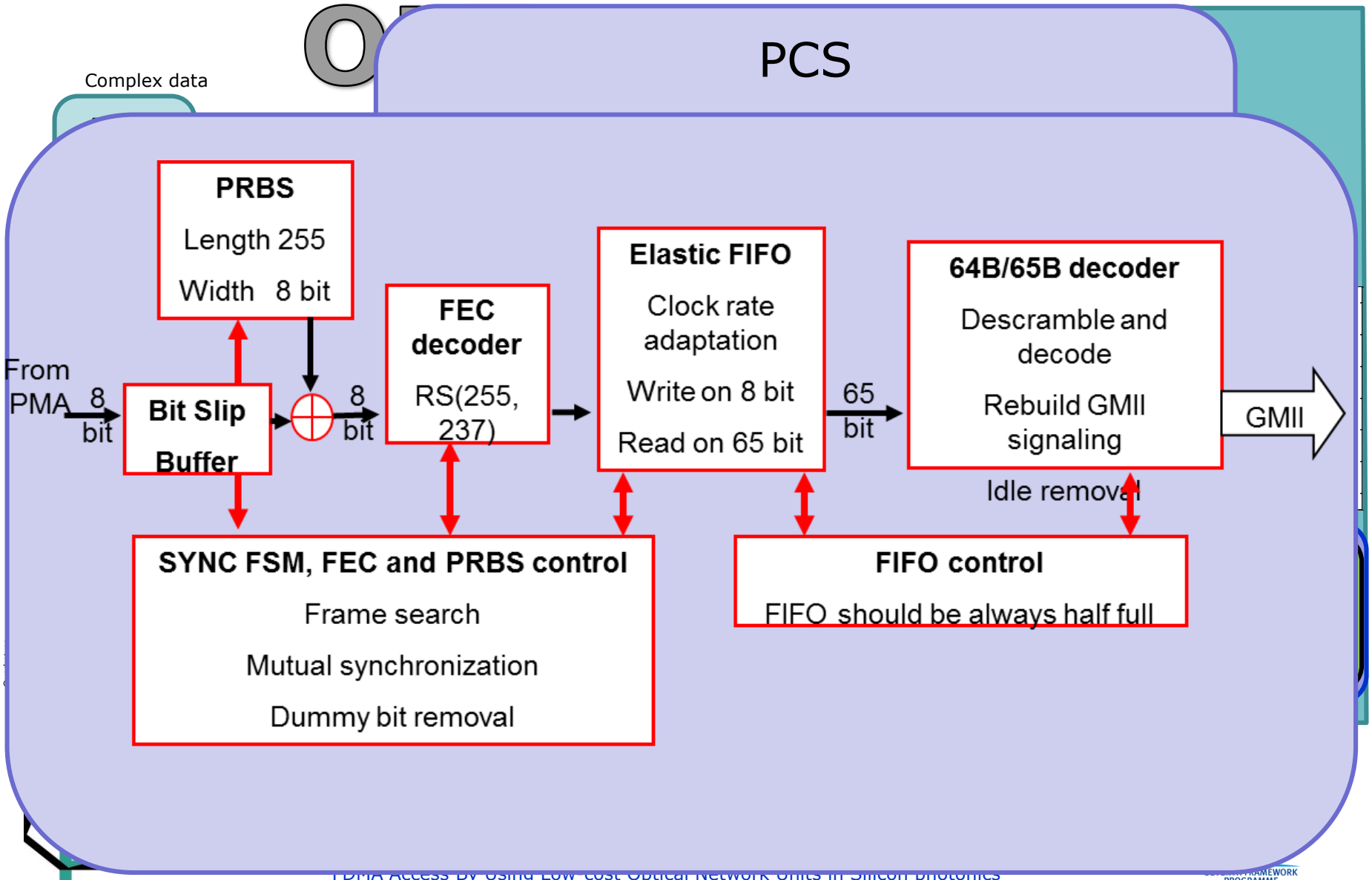
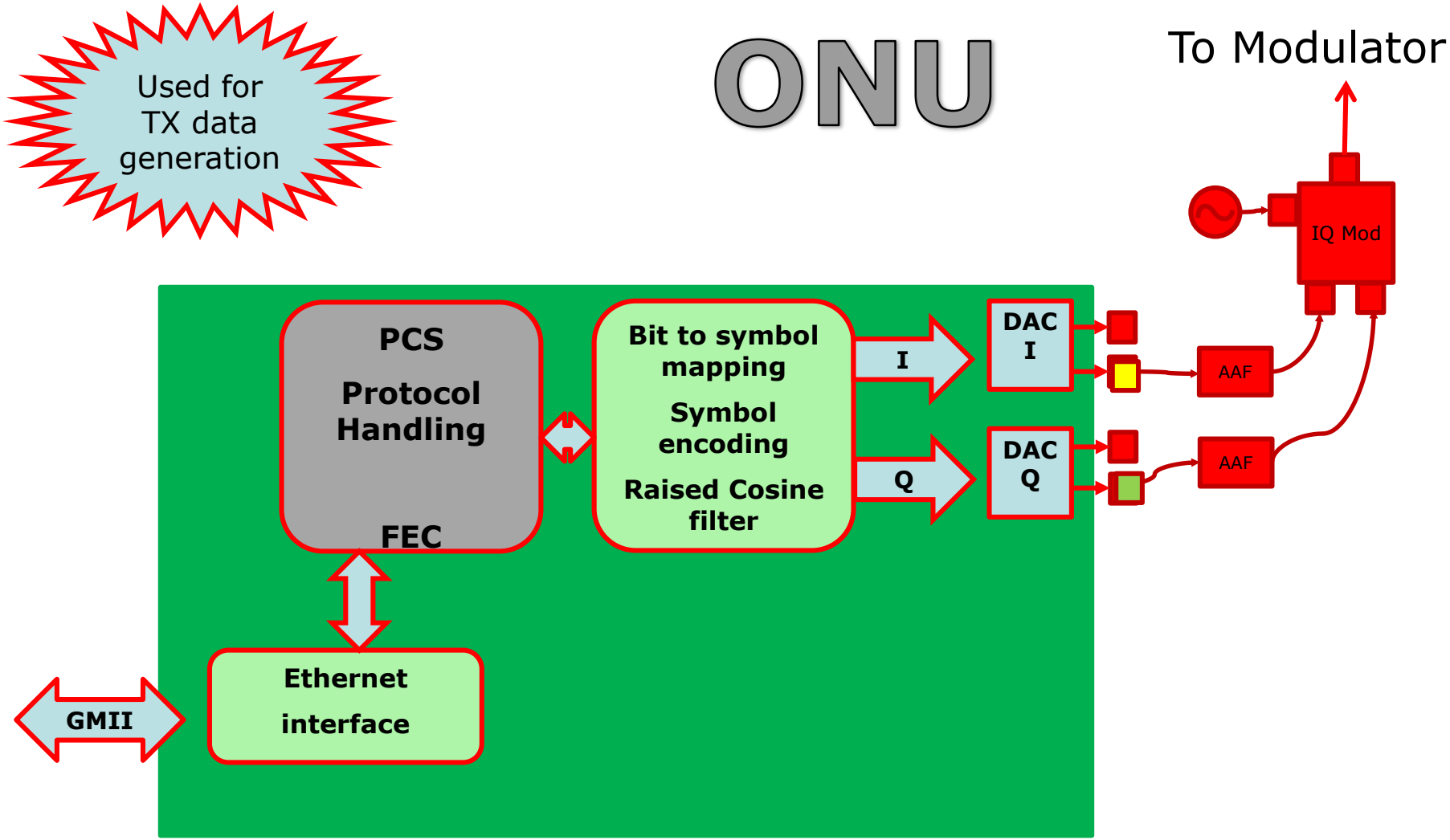
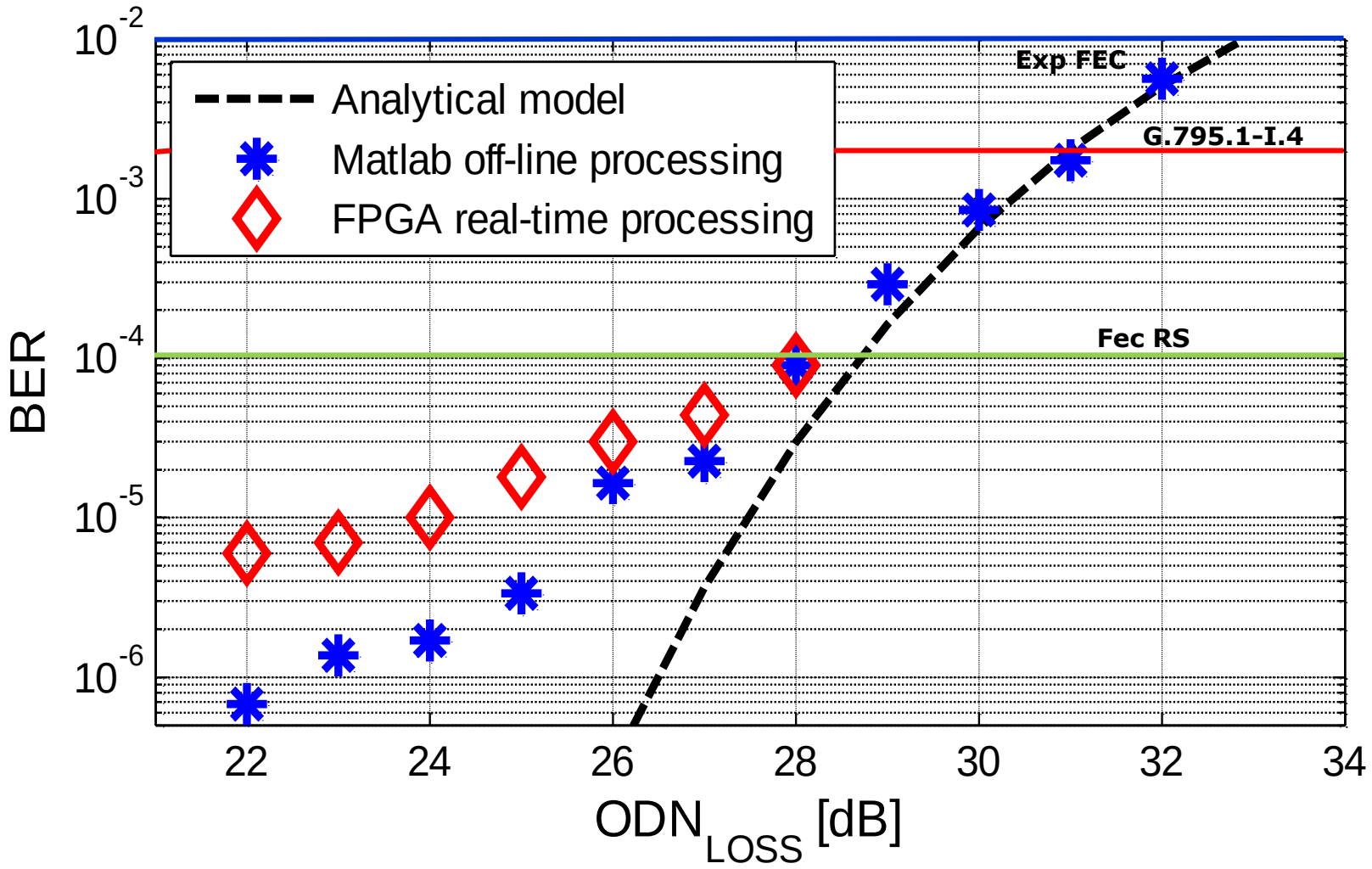
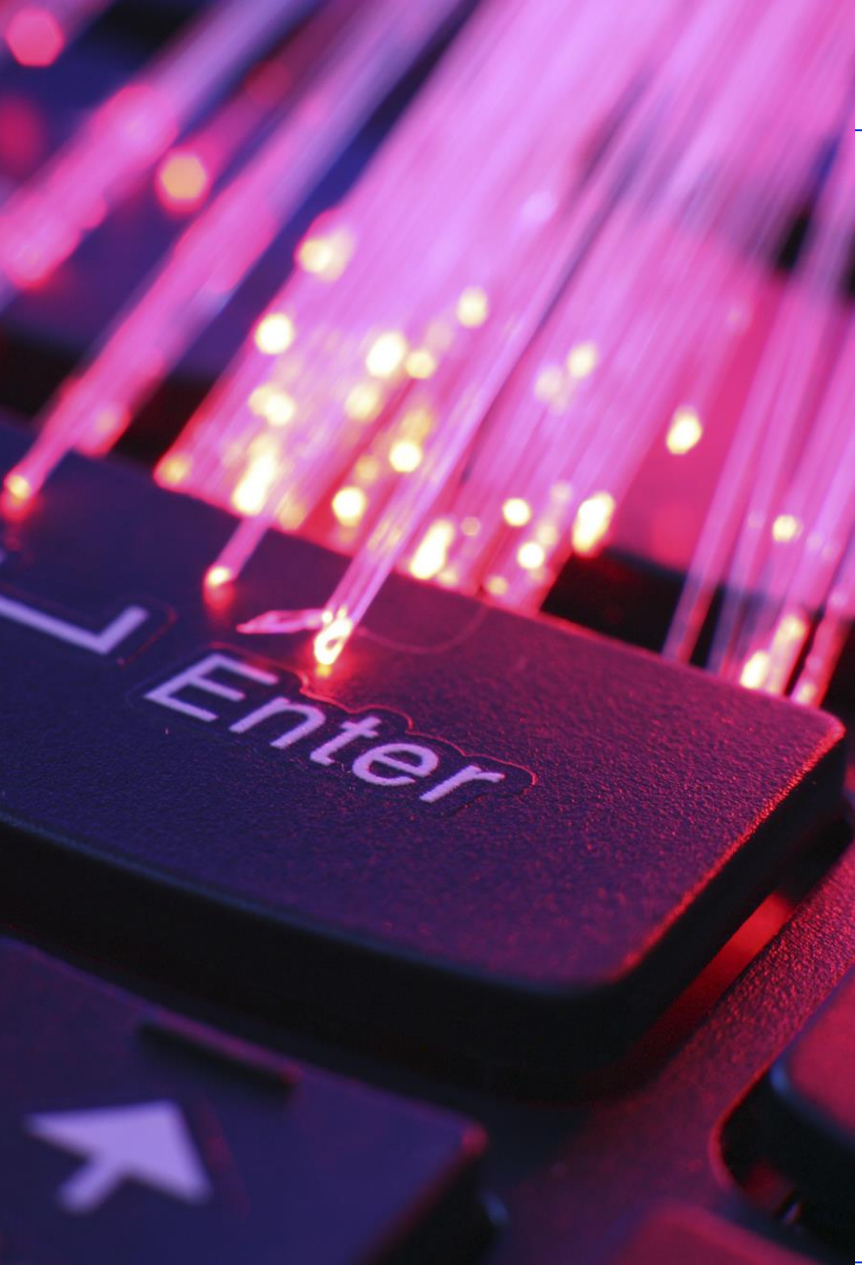


ONU TX block diagram



Real time vs DSP BER results





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We have presented the first results of real time data transmission on Fabulous upstream channel

The real time results compare well with theoretical and off-line DSP results.

1Gbit net rate, 37Km FW testbed fiber, 28dB ODN loss with implemented FEC

We are still investigating the floor present in our real time experiments

Acknowledgments

The research leading to these results has received funding from the European Community's Seventh Framework Programme FP7/2007-2013 under grant agreement n°318704, titled:

FABULOUS: "FDMA Access By Using Low-cost Optical Network Units in Silicon Photonics"

Experimental results obtained on Fastweb testbed

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