ROAD-NGN

Digital Signal Processing for FDMA-PON: Evaluation of Processing Complexity of Three Different Architectures

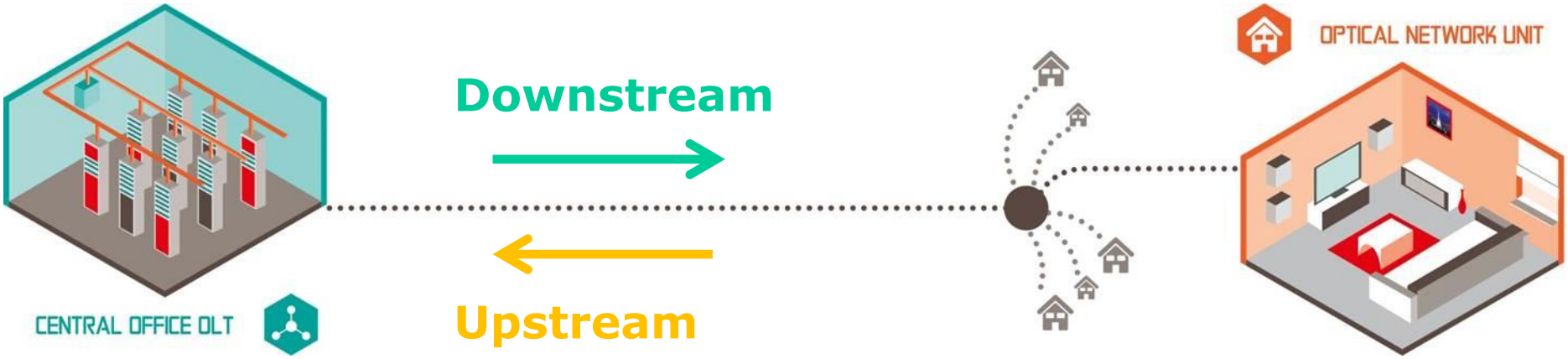
Roberto Cigliutti, POLITO

Roberto Gaudino, POLITO

Talk Agenda

- Motivations
- FDMA/OFDMA PON Case Studies
- Complexity Evaluations
- Conclusions

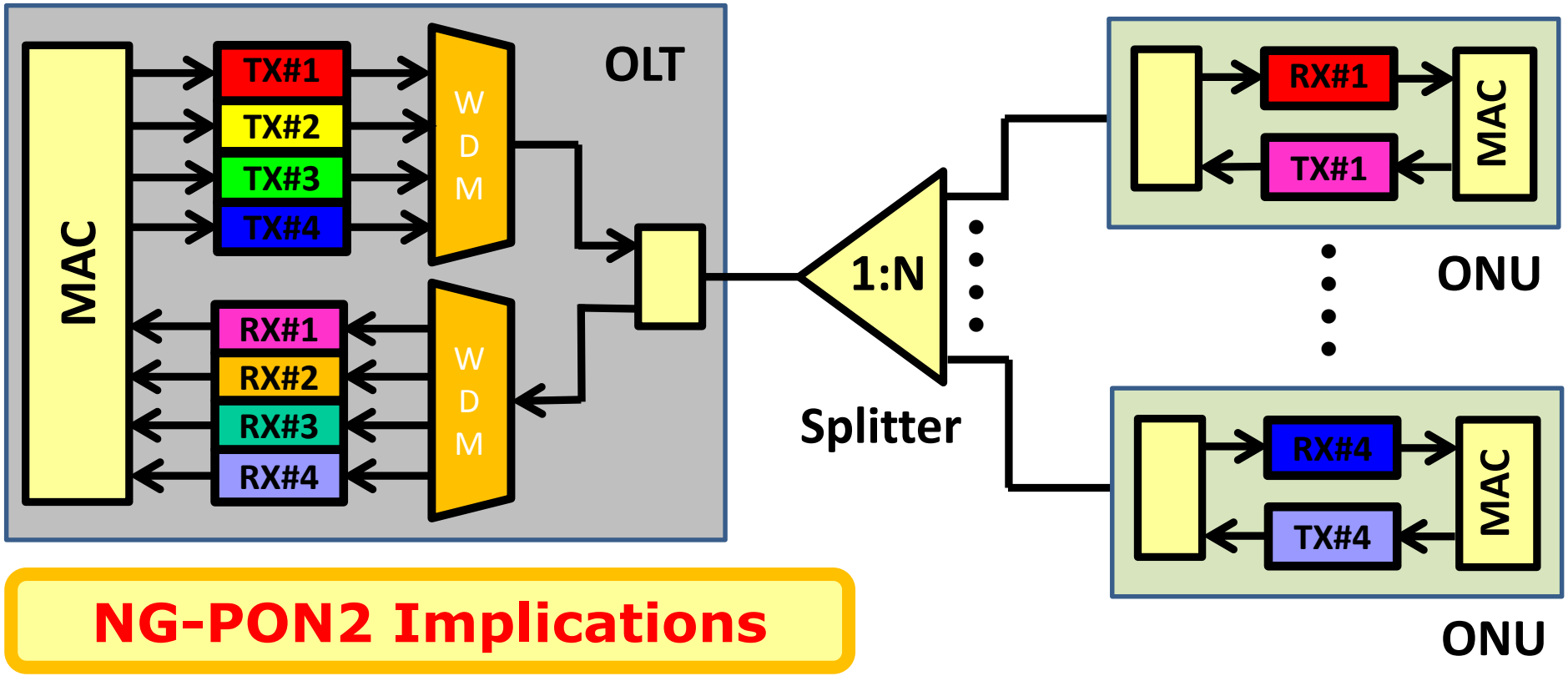
Toward New Generation-PONs



Latest PON ITU-T Standard

- ITU-T G.989 **NG-PON2** (**TWDM-PON**) (March 2013)
- PON Data Capacity:
  - 4λx10 Gbps **Downstream** and 4λx2.5 Gpbs **Upstream** (over up to 64 user)
  - Simultaneous use of **WDM** (4 λ) and **TDM** (Burst mode) technologies

Toward New Generation-PONs



NG-PON2 Implications

- **DS/US asymmetric** user data capacity (i.e. for 32 users: 1.25Gbps/312.5Mbps)
- "**Colored**" ONUs (ONUs are not interchangeable: i.e. 8-ONU/λ)
- In-service **synchronization** of the TDM ONUs

CMOS Technology Evolution

RELEASED FOR PRODUCTION

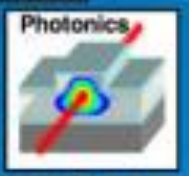
Innovation Enabled Technology Pipeline

Our Visibility Continues to Go Out ~10 Years

32nm	22nm	14nm	10nm	7nm	5nm
2009	2011	2013		2015+	

Manufacturing | Development | Research

Future Options



Latest Released Devices

45nm	28nm	20nm	16nm
SPARTAN	VIRTEX 7 KINTEX 7 ARTIX 7	VIRTEX UltraSCALE KINTEX UltraSCALE	VIRTEX UltraSCALE+ KINTEX UltraSCALE+

XILINX
ALL PROGRAMMABLE.

	Virtex-7 Family	Virtex UltraScale	Virtex UltraScale+
Logic Cells (K)	1,955K	627–4,433	690–2,863
DSP (Slices)	3,600	600–2,880	2,280–11,904
DSP Performance (GMAC/s)	5,335 GMAC/s	4,268	21,213

2x DSP Slices
2x Logic Cells
2x Clock Speed
4x DSP Performances

High-Speed & Low-cost DACs
f_s<1GS/s

Fujitsu Semiconductor Europe

Factsheet
LEIA
55 – 65 GSa/s 8-bit DAC

Ultra-High-Speed DACs
f_s>20GS/s

Facts,Consequences &Open Questions

FACTS

- New high-speed electronic devices are today available.

CONSEQUENCES

- A 10GHz analog processing bandwidth can be considered almost “a commodity”.
- Electrical FDM-PON can be a realistic solution for future NG-PONs.

OPEN QUESTIONS

- *Can a data capacity up to 40 Gb/s be handled at the OLT?*
- *Which is the most promising (cost, complexity) solution?*

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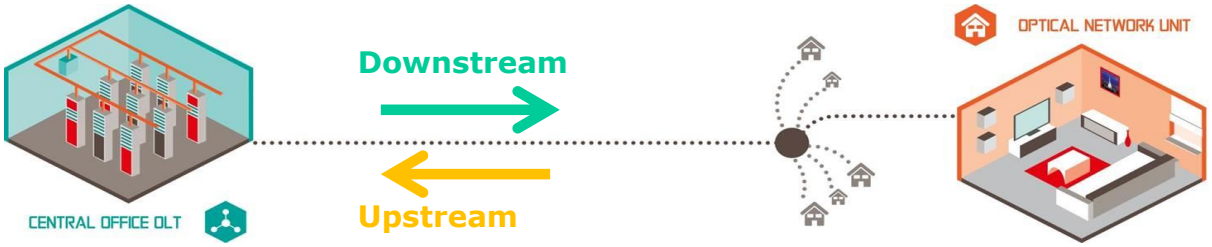
Toward New Generation-PONs



Improving NG-PON2

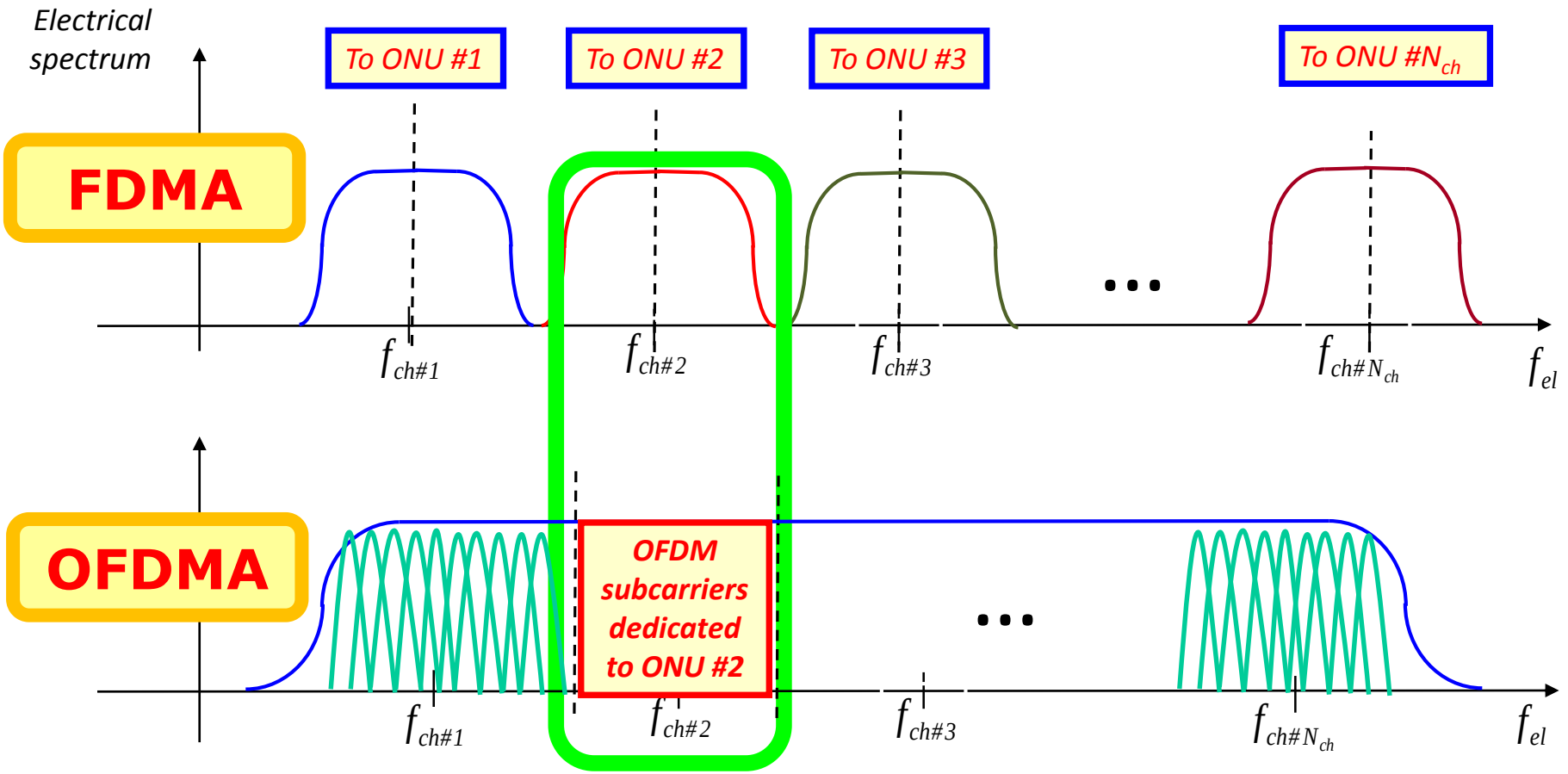
- **DS/US symmetric** (1 Gbps/user) over a **single wavelength**
- Simplification of the ONUs operations

DOWNSTREAM CASE STUDY:

- Delivery of multilevel signals (1 Gbps/user per 32 users)over a **single wavelength** over the **same ODN classes** of the NG-PON2
- Use of the **Electrical FDM-(A)ccess** Technology (i.e. Electrical FDM) with **SUBBAND DETECTION** at ONUs
- Mandatory use of "**low-cost**" HW (DAC & DSP) for the ONUs

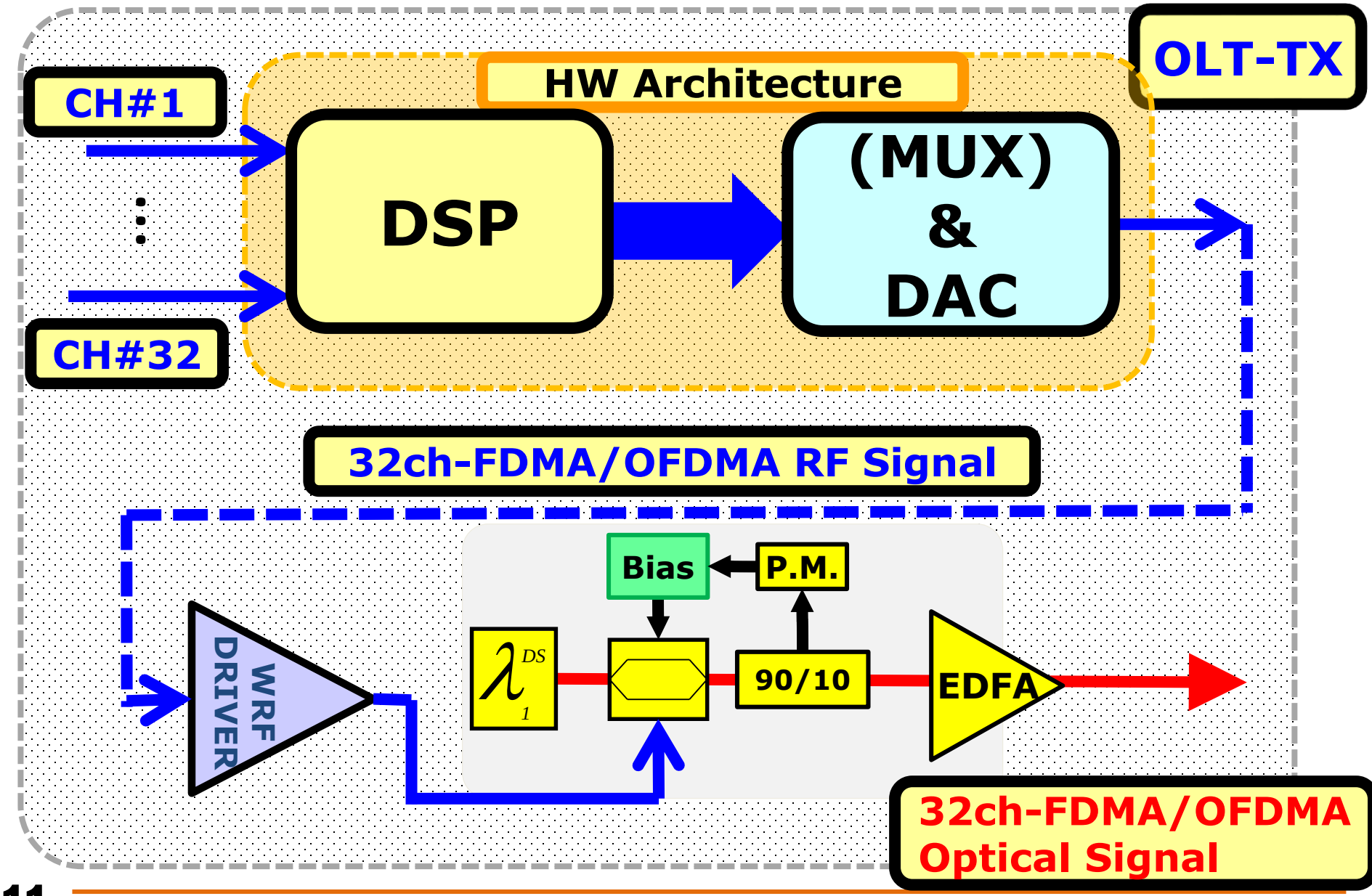
Sub-Band Detection

- Subcarrier Multiplexing for Sub-band Detection



More compact frequency Spectrum

OLT TX Architecture



Electrical FDMA vs. OFDMA

FDMA Approach:

- **User Channel System Parameters**

  16QAM @ R_s=275MBaud (incl. FEC); 10% Nyquist spectrum roll-off, BW≈9.8GHz

- **Sub-band DSP also in OLT**
  - Architecture #1 – Mixed Analog/Digital
- **Full-band DSP**
  - Architecture #2 – Full Digital

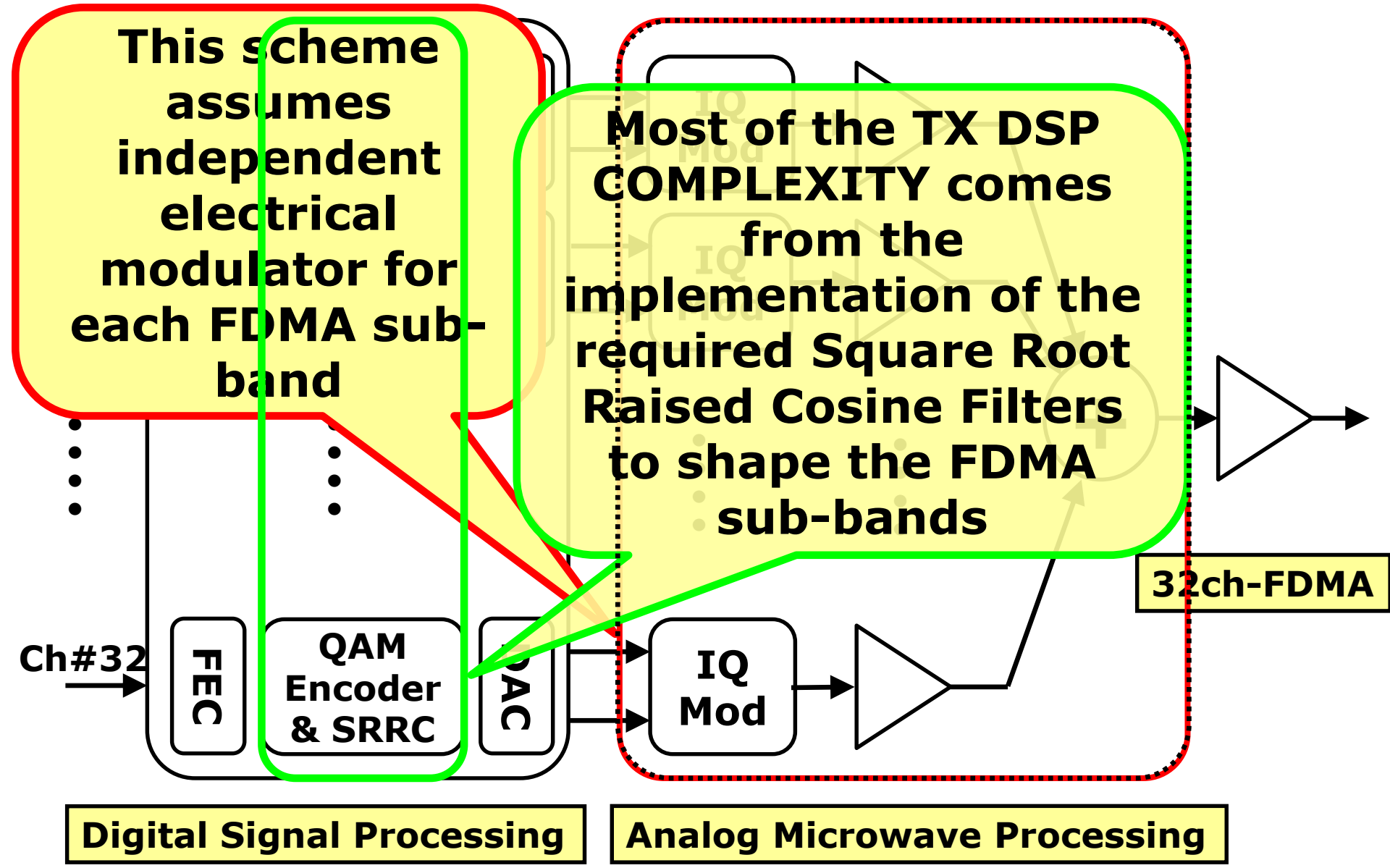
OFDMA Approach:

- **User Channel System Parameters**

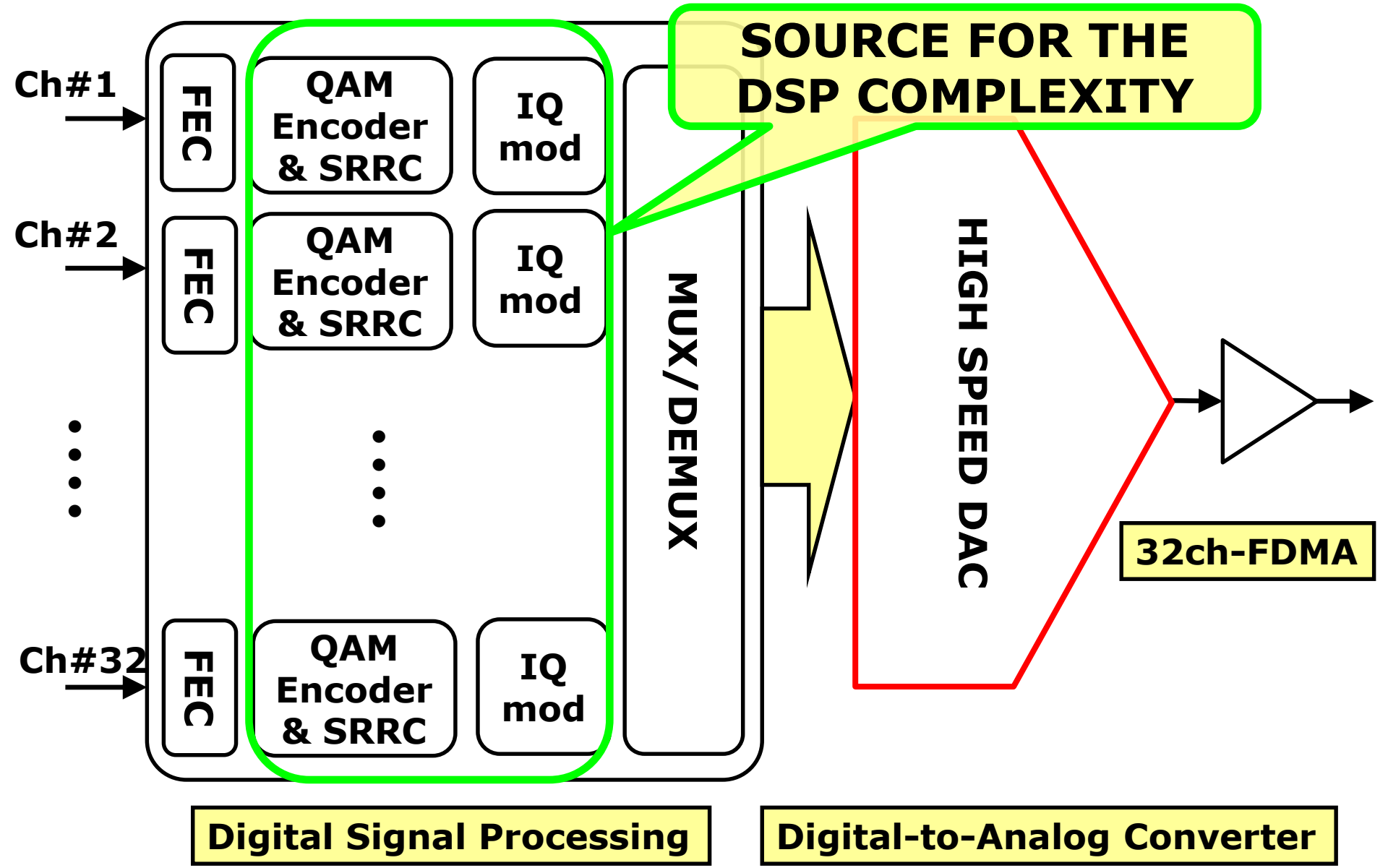
  10 OFDM Subcarriers/channel; each subcarrier 16QAM @ R_s=27.5MBaud (incl. FEC), BW≈8.8GHz

- **Full-band DSP** (Sub-band OFDM is not practical)
  - Architecture #3 – Full Digital

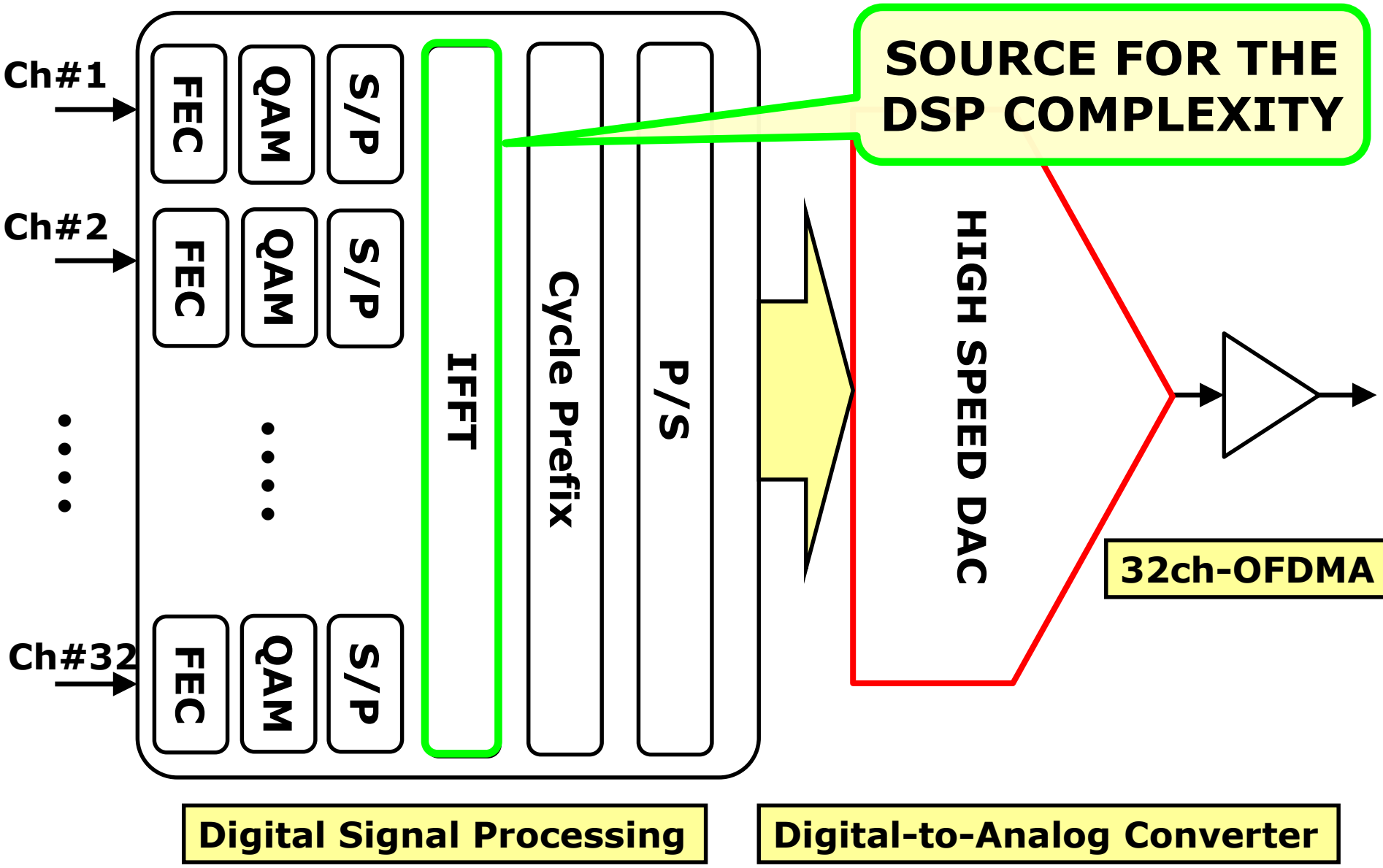
FDMA #1: Mixed Digital/Analog Sol.



FDMA #2: Full Digital Solution



OFDMA: Full Digital Solution



HW/DSP Solutions: FDMA vs. OFDMA

	FDMA Architecture #1 (Mixed Dig./Analog)	FDMA Architecture #2 (Full Digital)	OFDMA Architecture (Full Digital)
DSP	**Entry level FPGA/ASIC** (Fs≥555.5 MHz) ☺	**High-End FPGA/ASIC** (Equiv. Fs≥18.026 GHz) 😐	**High-End FPGA/ASIC** (Equiv. Fs≥18.026 GHz) 😐
DAC	**N≤32 x Low-Cost CMOS** ☺	**1x High Perfor. CMOS** 😐	**1x High Perfor. CMOS** 😐
Analog	**I/Q mixers, RF Amplifiers, 1:32 coupler** ☹ **(Critical Design)**	**RF Amplifiers only** ☺	**RF Amplifiers only** ☺
Operation	High power dissipation (analog HW) ☹ but scalable w.r.t. the active channels # ☺	Possible power dissipation scaling w.r.t the # of active users ☺	DSP scaling for the # of active users not possible in principle (Fixed IFFT size) 😐

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DSP Blocks & Parameters

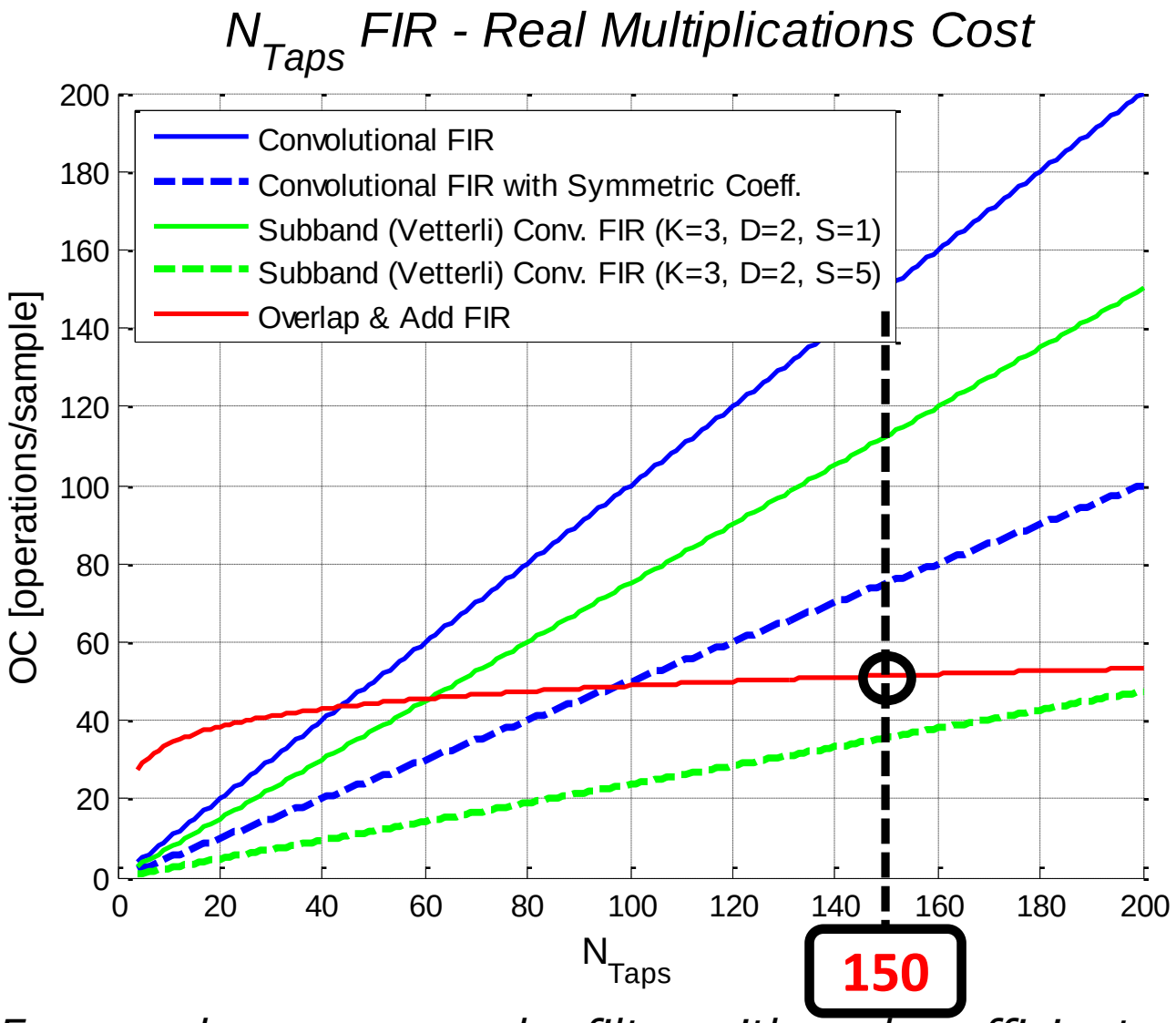
FDMA Architectures

- **SRRC FIR Filter (**N_{taps}=150):
  Overlap&Save – with 2048 pts/block @ f_s=550 MSample/s
- **Upsampling**:
  Cascaded-Integrator-Comb (CIC) interpolating filters
  (no multiplications/sums required)
- **I/Q modulation:**
  classical sin() /cos() multiplication + 1 sum @ f_s=19.8 GSample/s

OFDMA Architectures

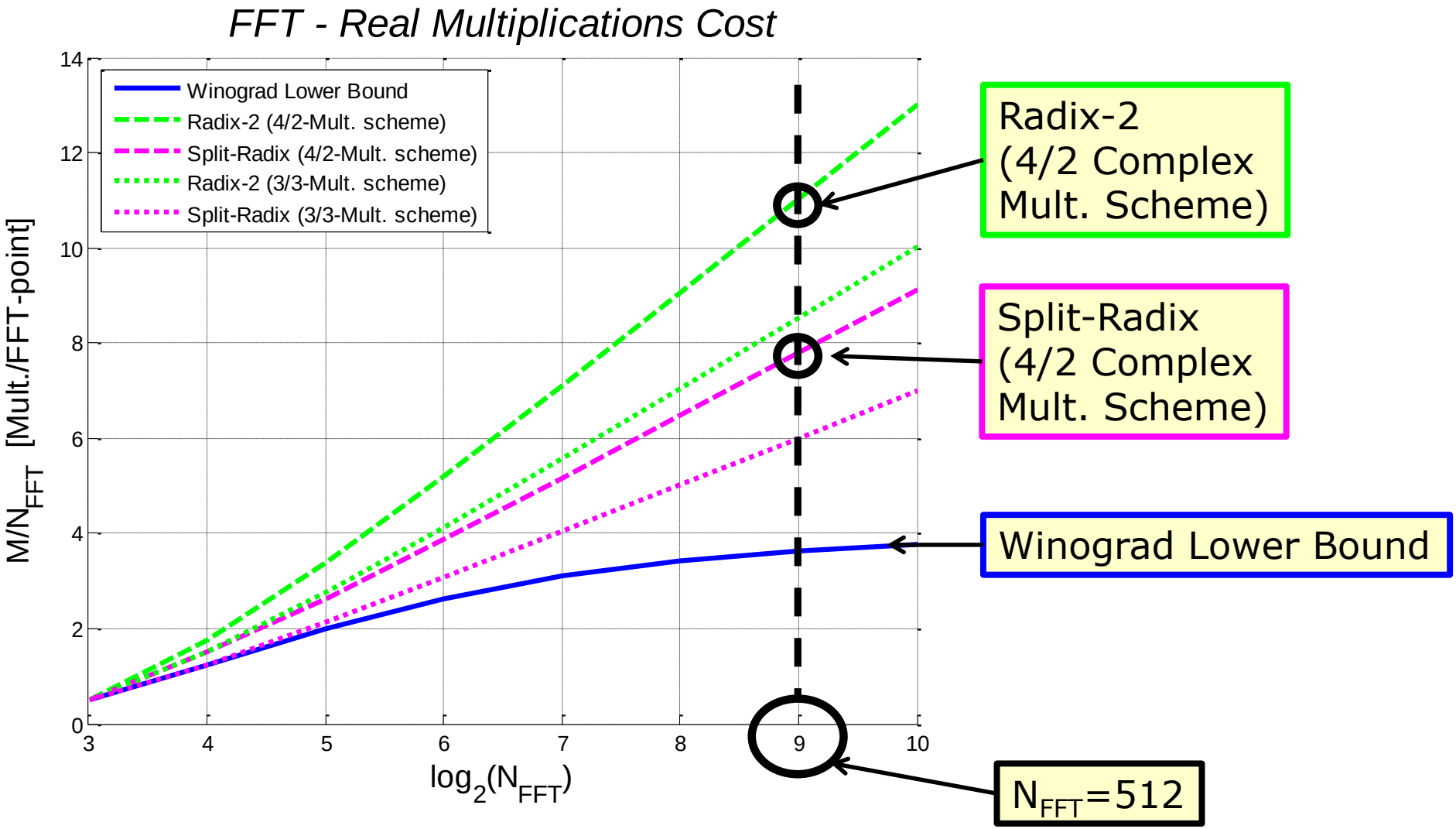
- **IFFT** (size =1024 pts for BW≈10GHz signal):
  Optimized Radix-2 or Split-Radix FFT Algorithms
  (Real-valued signal ⇒ halves required FFT size to 512pts)

FIR Filter Algorithms



- *For a real sequence and a filter with real coefficients.*

FFT/IFFT Algorithms



- *Number of DSP Multipliers ≤ Number of Algorithm Multiplications*

Computational Complexity

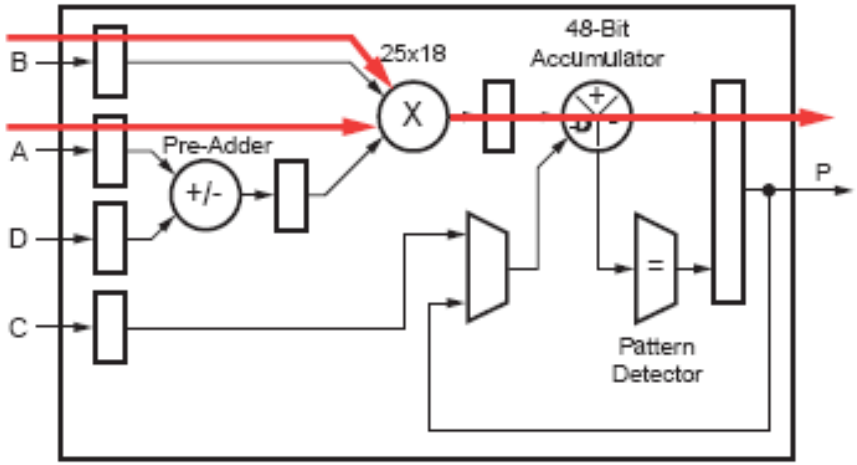
	Real Multiplications [Operations/bit]	Real Sums [Operations/bit]
FDMA Architecture #1 (**Overlap & Save** FIR N_{taps}=150 FFT Block $N_{FFT}=2^{11}=2048$)	***≈ 72.09***	***≈ 102.13***
FDMA Architecture #2 (**Overlap & Save** FIR N_{taps}=150 FFT Block $N_{FFT}=2^{11}=2048$)	***≈ 108.20***	***≈ 192.40***
OFDMA-R2 Architecture (**Optimized Radix-2 FFT** N_{FFT}=512, Subcarriers # N_{SC}=10)	***≈ 44.09***	***≈ 96.03***
OFDMA-SR Architecture (**Optimized Split-Radix FFT** N_{FFT}=512, Subcarriers # N_{SC}=10)	***≈ 31.16***	***≈ 88.91***

- Symbol Rate: R_s=275 Mbaud (Including FEC)
- QAM order: M=16,
- Number of Mux Channels: N_{ch}=32

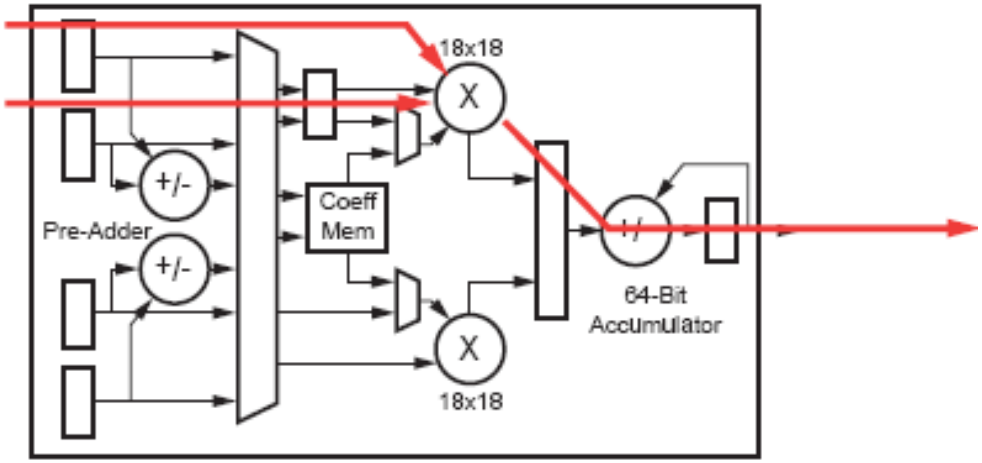
FPGA Resources: Slices

Multiplications & Sums ⇒ Physical Multipliers & Adders

Virtex-7 FPGA DSP48E1 Slices

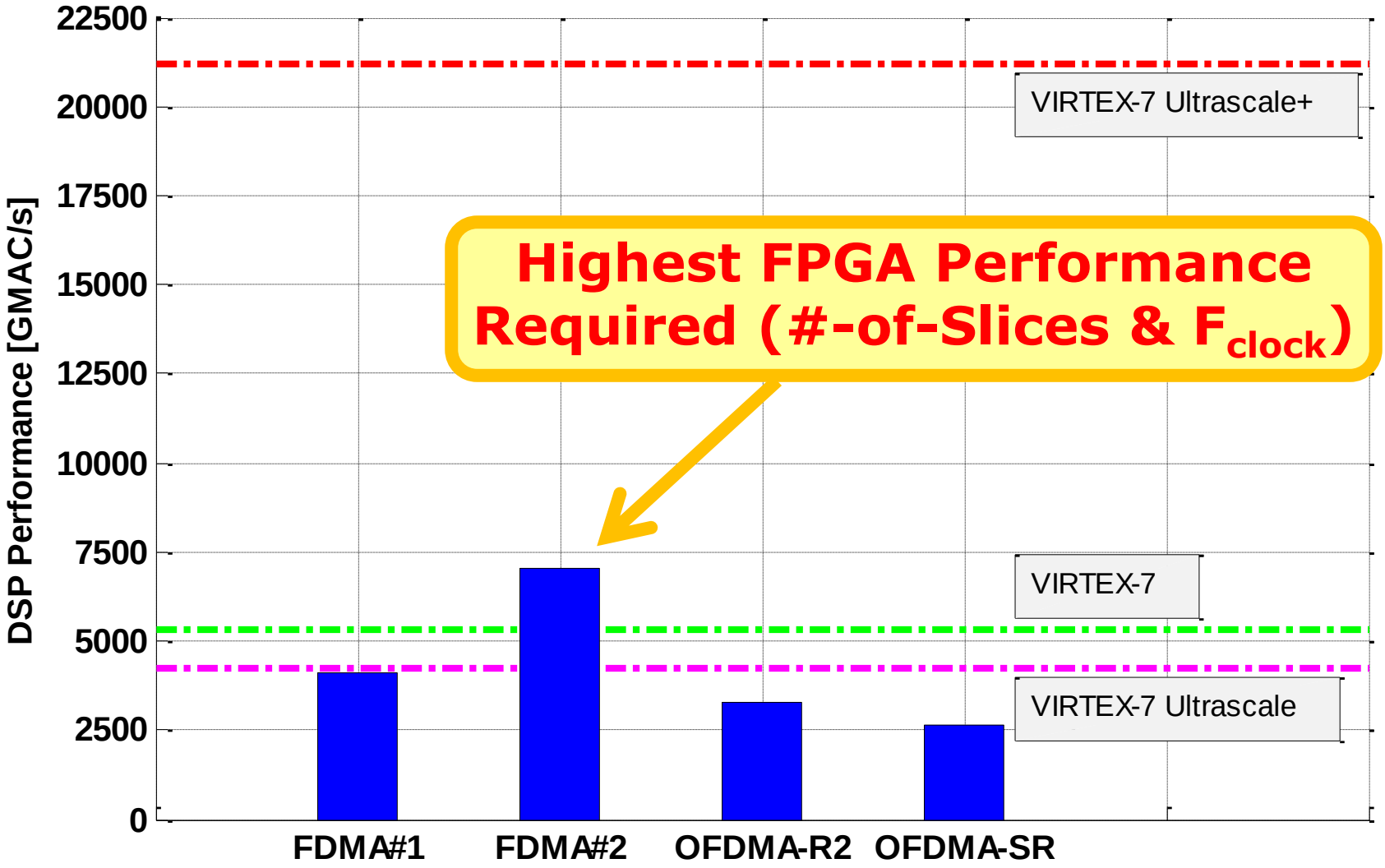


Stratix V DSP Block



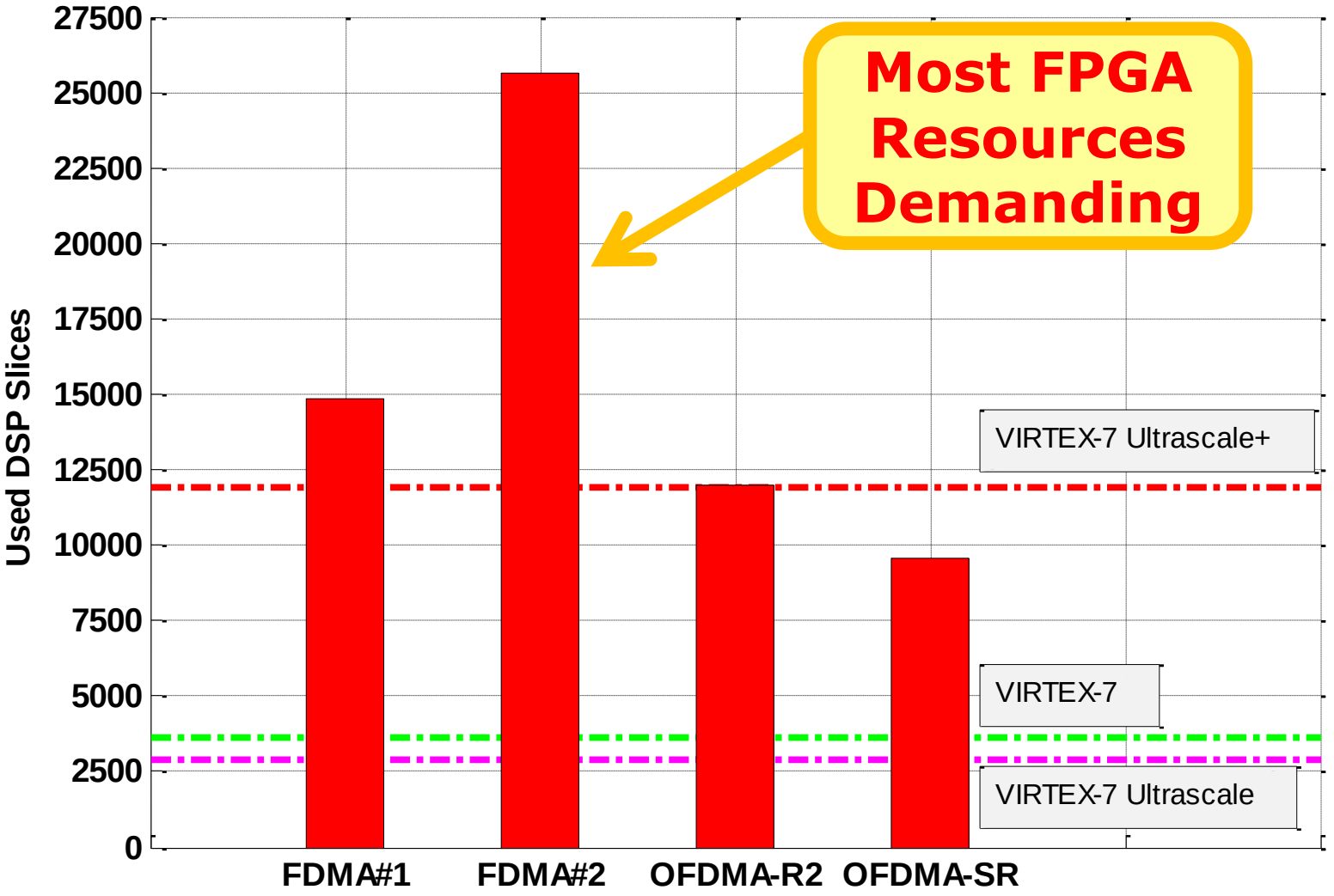
- 1 Multiply-and-Accumulate (MAC) unit (Slice or Block) can be used for: **1x18bit Adder** or **1x18bit Multiplier**
- Computational complexity in FPGA/DSP:
  - **Overall DSP size** (number of "DSP Slices or Blocks"
  - **Computation Performance** (MAC operations-per-second i.e MAC/s)

FPGA-DSP Performances



1 MAC =1 Multiply-and-Accumulate DSP Unit

FPGA Resources Usage



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Conclusions

- The **OFDMA approach** results to be advantageous w.r.t. the DSP implementation in FPGA (Particularly using Split-Radix based FFTs).
- All **FDMA approaches** are less efficient from the DSP complexity point-of-view.

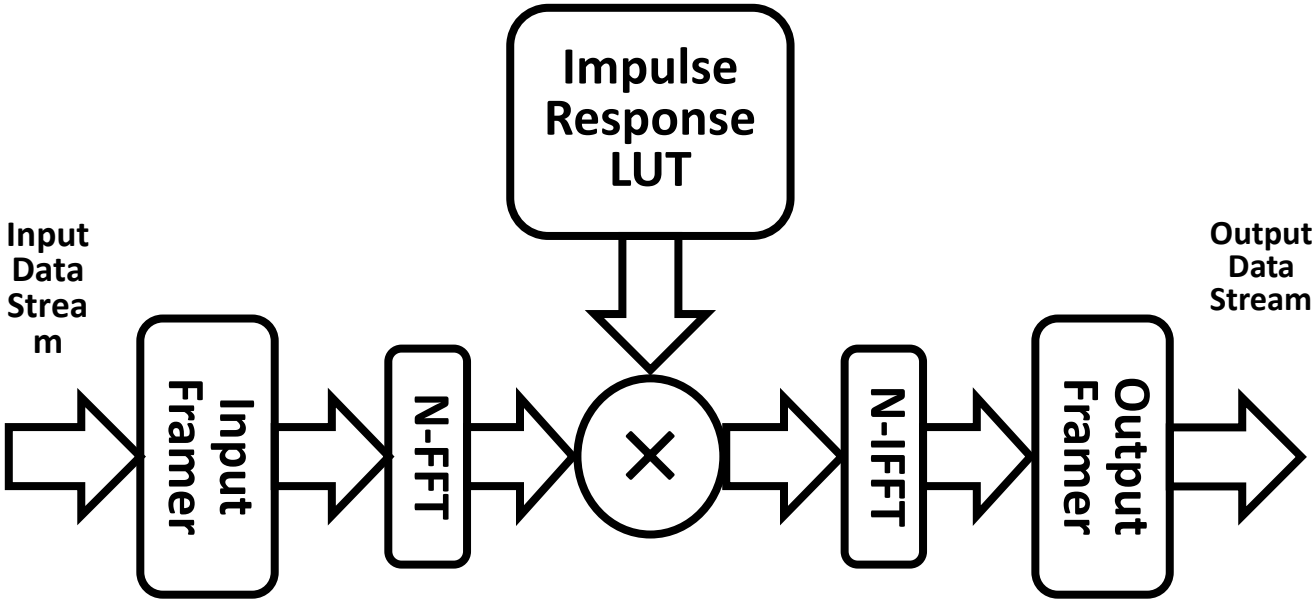
- Nevertheless:
  - the **"Full Digital" FDMA approach** allows the implementation of **power saving** features for reduced user numbers ⇒ **OPEX saving**
  - The **"Mixed Digital/Analog" FDMA approach** is the only solution that does **not** require **very fast DACs** ⇒ actually the **cheapest solution**.

http://www.roadngn.uniroma3.it/index.html

THANK YOU FOR YOUR ATTENTION

BACK-UP SLIDES

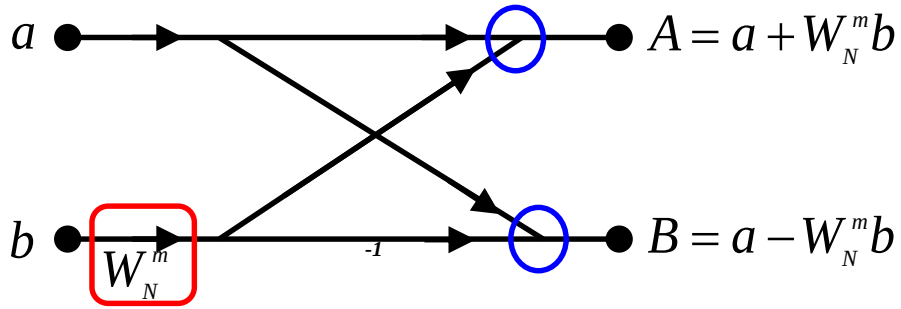
- **Convolution Filter**
  - Overlap&Save Algorithm:



- **Pros and Cons**
  - Compromise between complexity and I/O latency
  - Requires high FFT size for efficiency (i.e. 2048pts for 150 Taps)

- **Optimized Radix-2**

Classical Cooley-Turkey FFT w/o Trivial Multiplications (i.e. Twiddle factors $(W_N)^m = +1, -1, +i, -i$).



"Butterfly" computation unit for Radix-2 algorithms

- **Optimized Split-Radix**

Modification of the Cooley-Turkey FFT using multiple order Radix "Butterflies" (i.e. Radix-2, 4, 8) for complexity optimization.

Both algorithms are suitable for the efficient implementation in VLSI/FPGA (Hardware optimization $\Rightarrow$ not included in this analysis)