Silicon Photonics and FDMA-PON: Insight from the EU FP7 FABULOUS Project

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FP7-ICT-2011-8 Challenge 3.5 – STREP project n. 318704 – FABULOUS

FDMA Access By Using Low-cost Optical Network Units in Silicon photonics

The ideas behind Fabulous

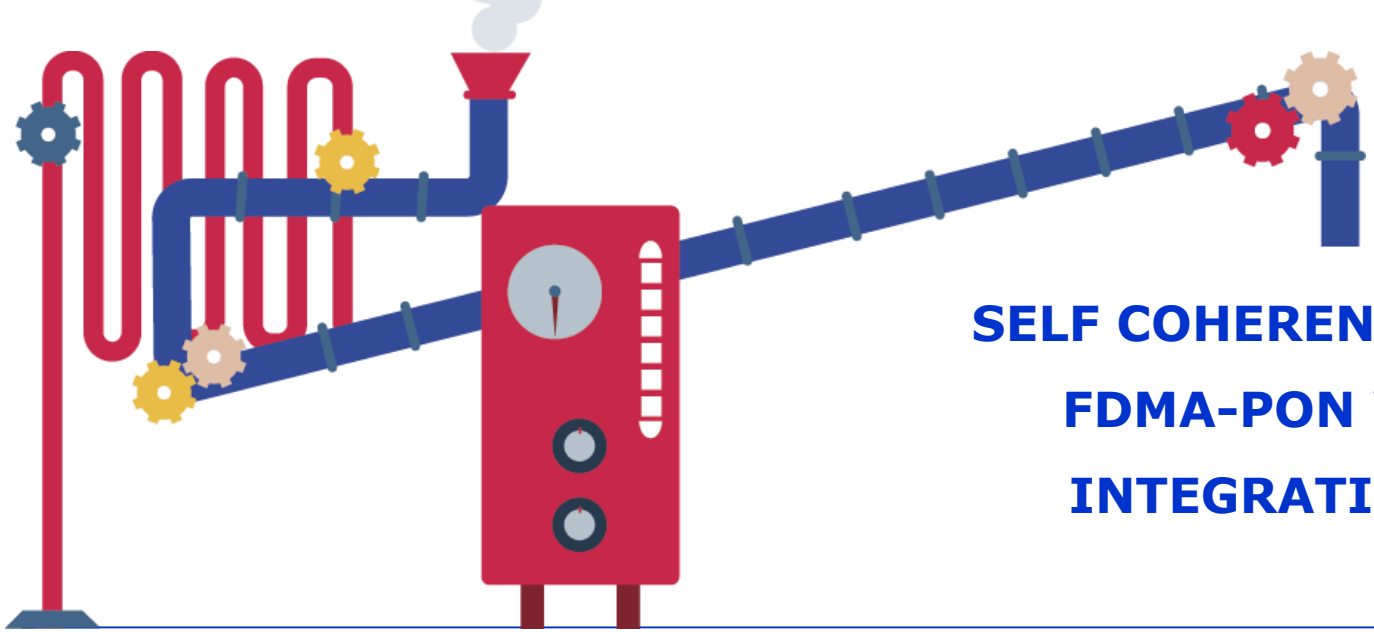
Flexible network

High capacity

ITU-T ODN compliant

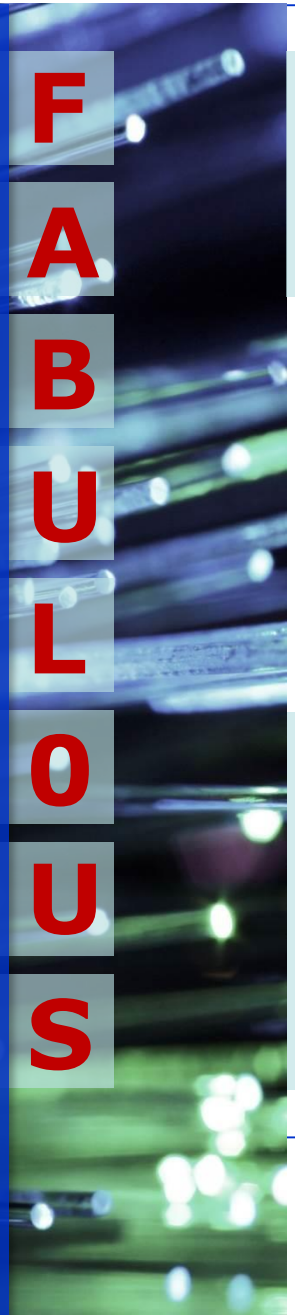
High level of optical integration

No uncontrolled λ at ONU switch-on



SELF COHERENT REFLECTIVE FDMA-PON WITH ONU INTEGRATION ON SiP

FABULOUS at-a-glance



F A B U L O U S

DMA ACCESS Y SING OW-COST PTICAL NETWORK NITS IN ILICON PHOTONICS

FP7-ICT-2011-8 – Objective 3.5: Core and disruptive photonic technologies

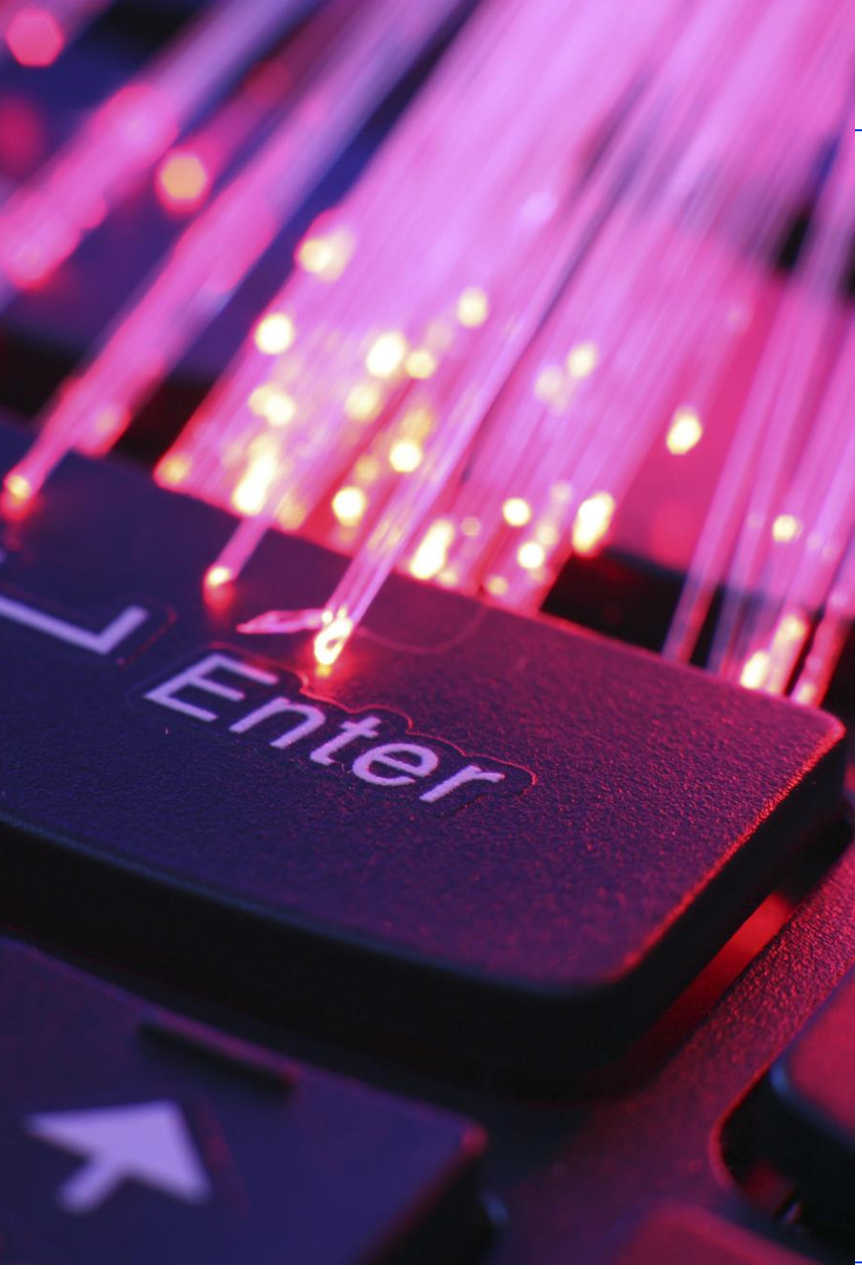
ARCHITECTURE

SYSTEM PARAMETERS

"Application-specific photonic components and subsystems"

"For access networks, the goal is affordable technology enabling 1-10 Gb/s data-rate per client"

NEW COMPONETS

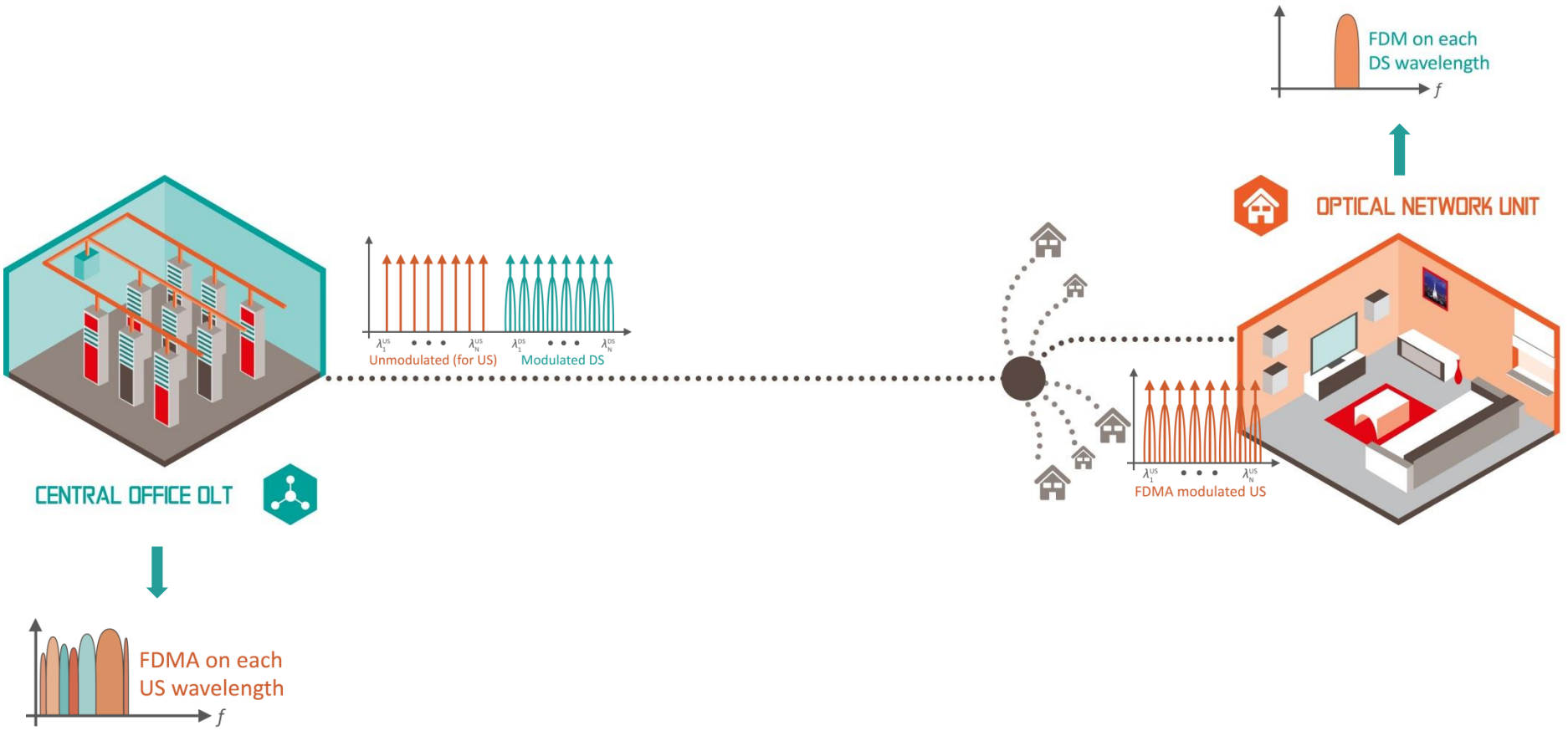


SUMMARY

- **Concept description: architecture and components**
- **Performance assessment with discrete components**
- **Status of components development**
- **Conclusions**

The general architecture

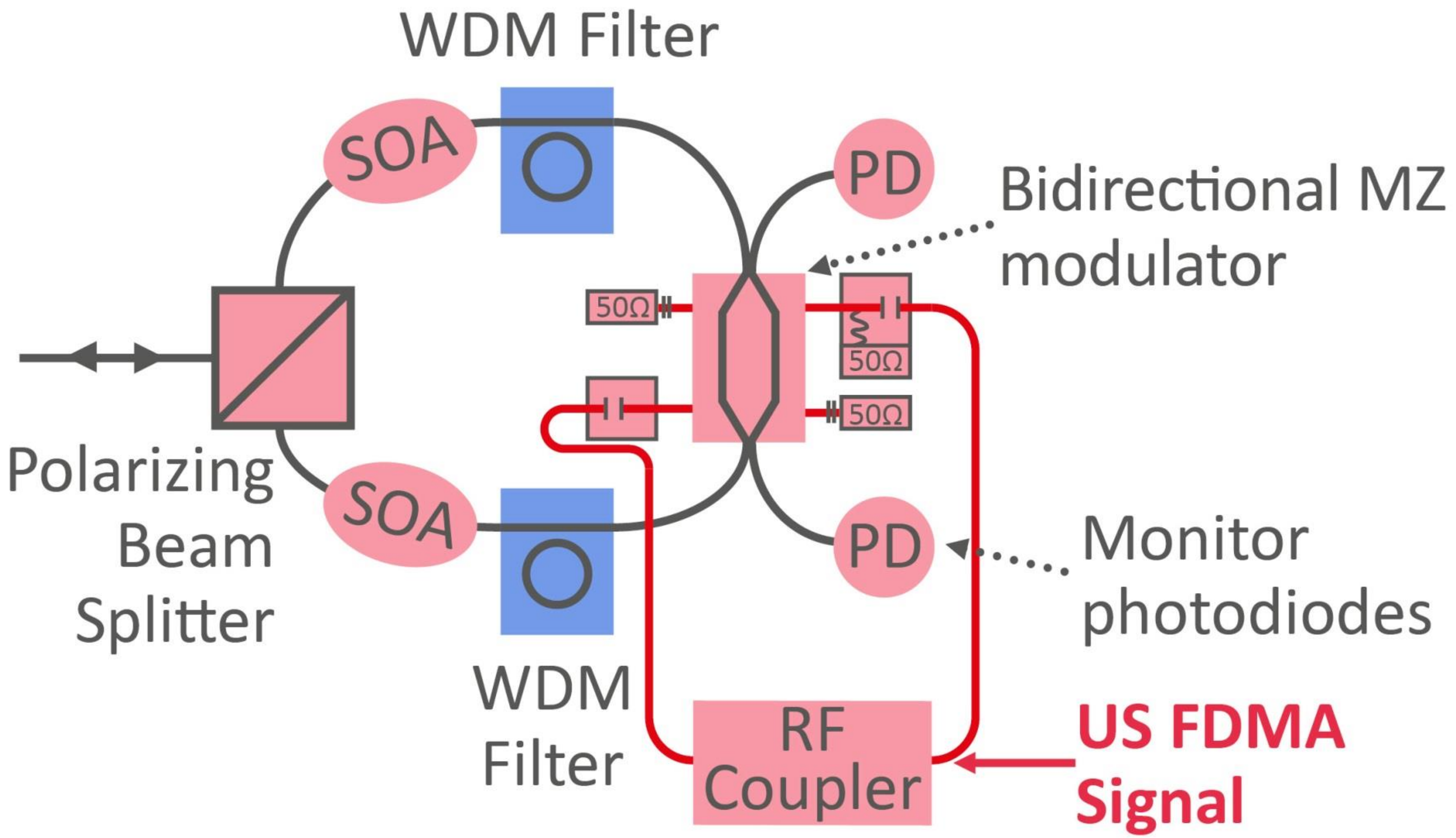
Reflective WDM PON based on FDM / FDMA



The ONU

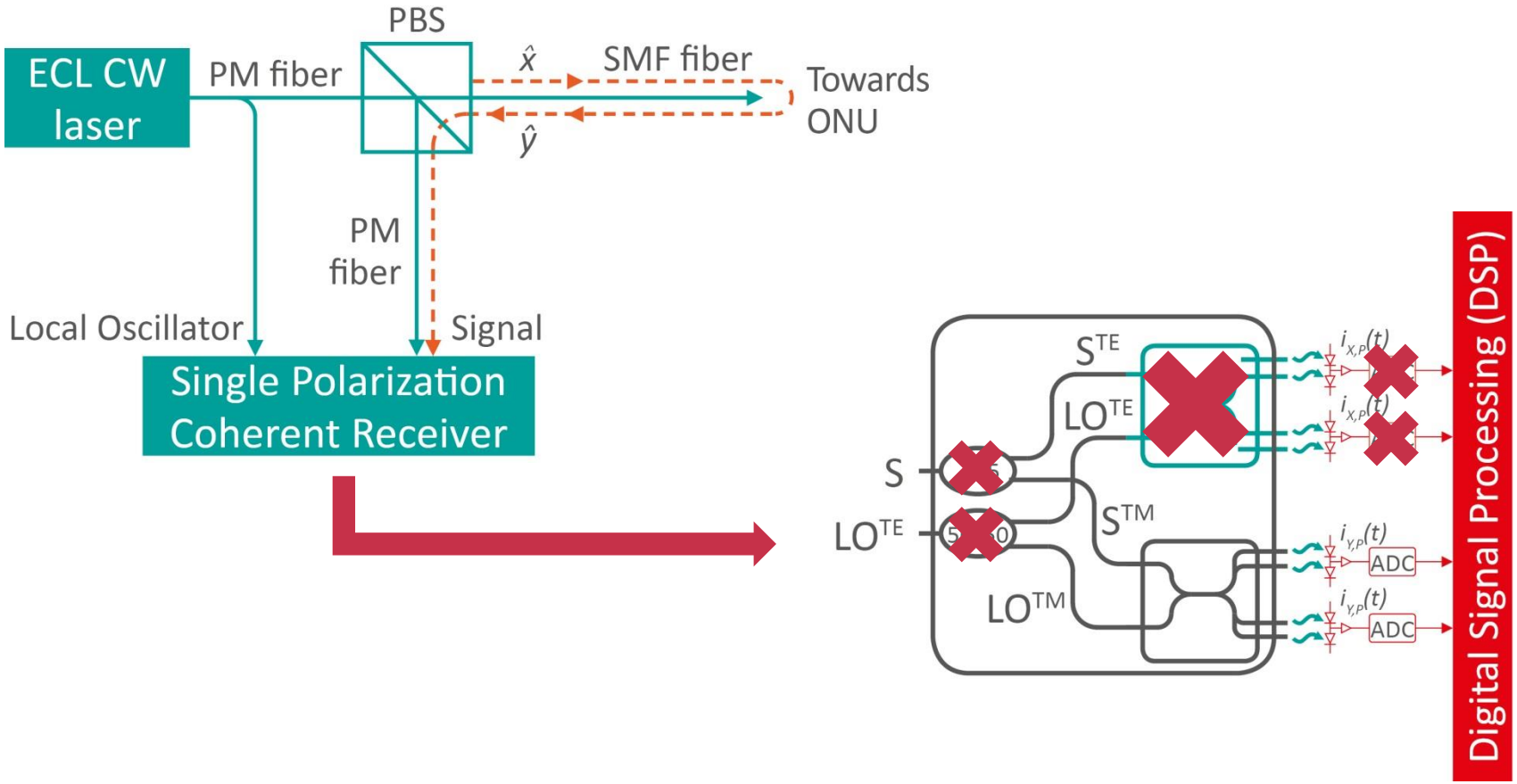
The ONU of the project is designed to be a Silicon Photonics PIC

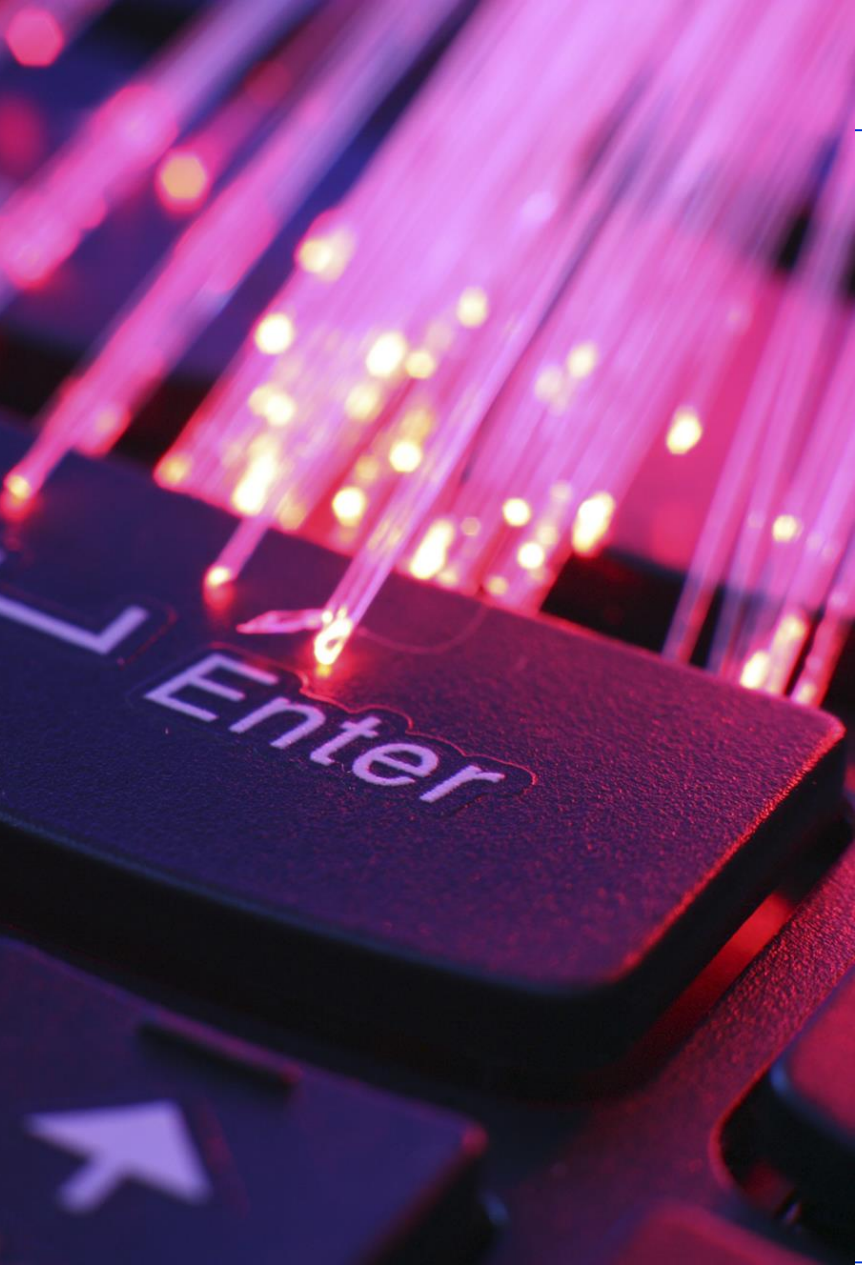
Purpose: reflects the signal, modulates it and performs 90° polarization rotation



The OLT

Polarization rotation allows symplified coherent detection at the OLT





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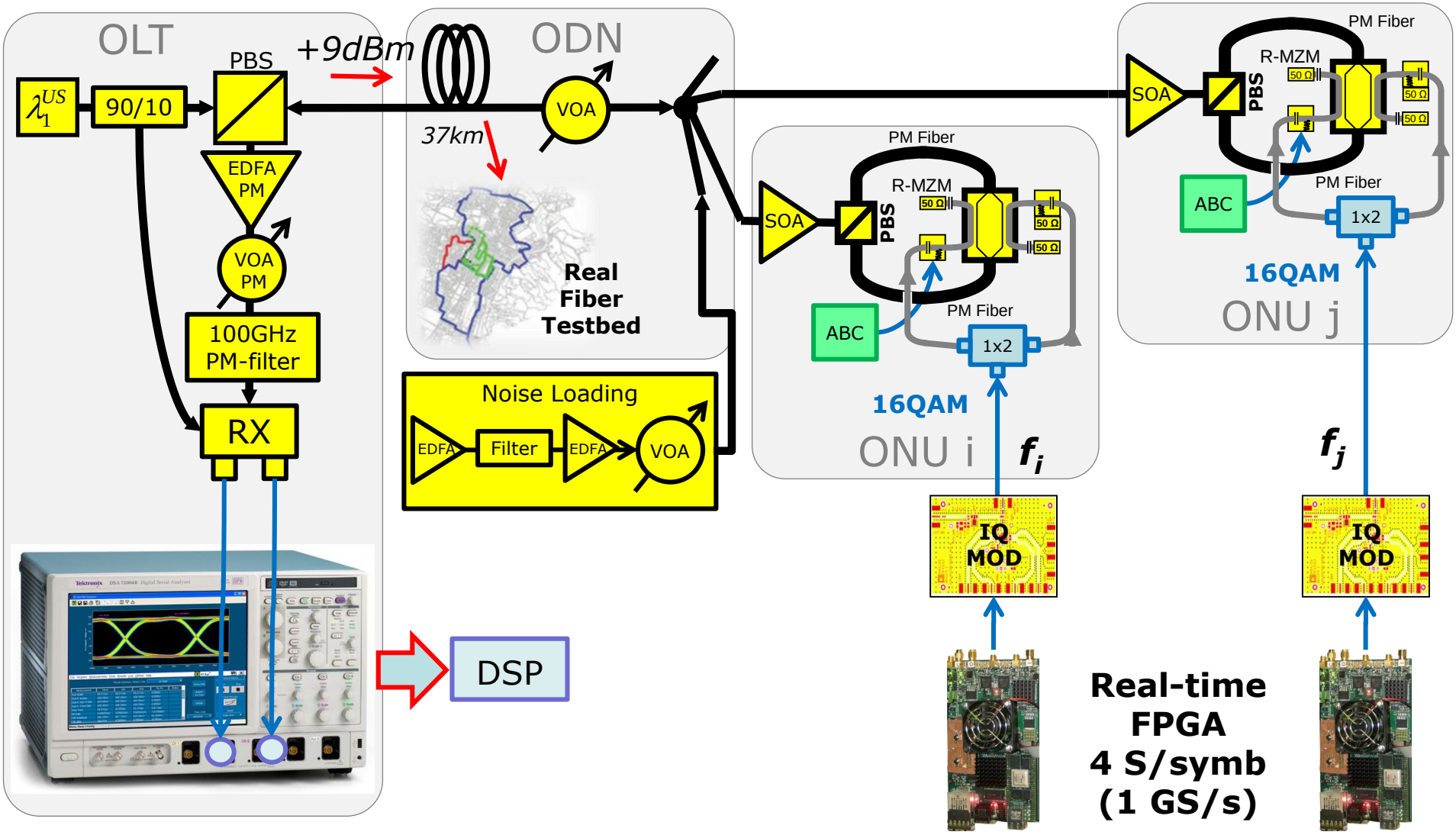
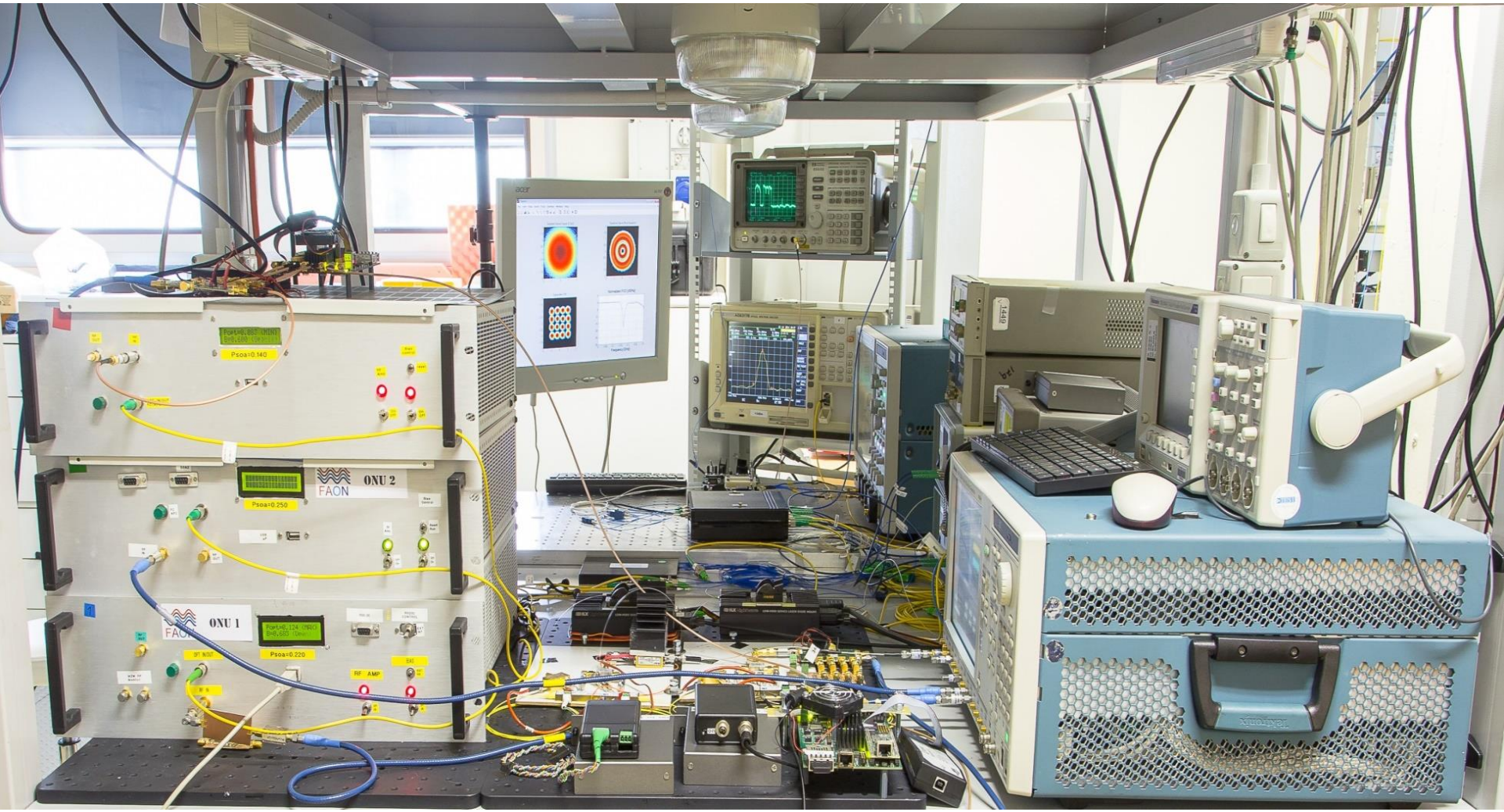
Upstream setup



Upstream setup



Targets for this set of experiments

DATA RATE PER USER SET AT 1 GBPS

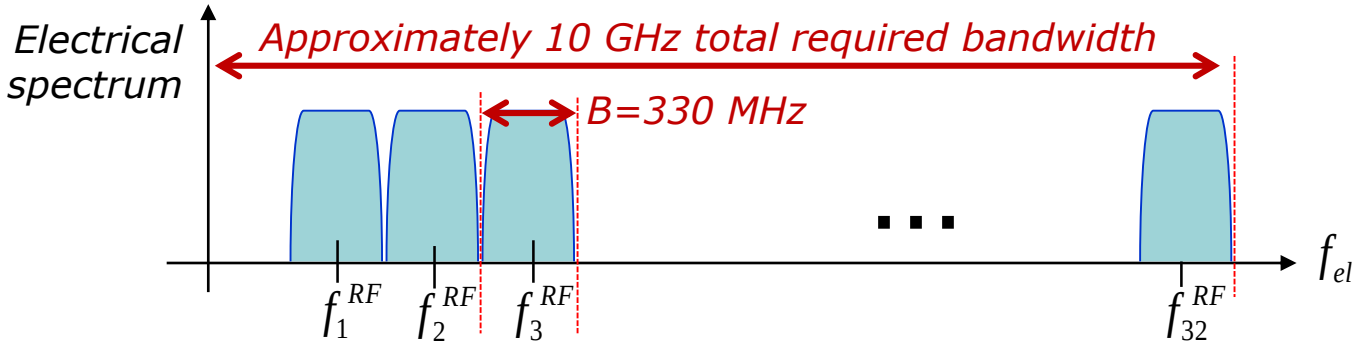
- (net data rate, giving a gross rate of 1.2 Gbps including FEC, overhead and line coding)

MODULATION FORMAT SET AT 16-QAM

- Raised cosine spectrum, roll-off=0.1
- Requires *B*~330 MHz per user

32 USERS PER WAVELENGTH

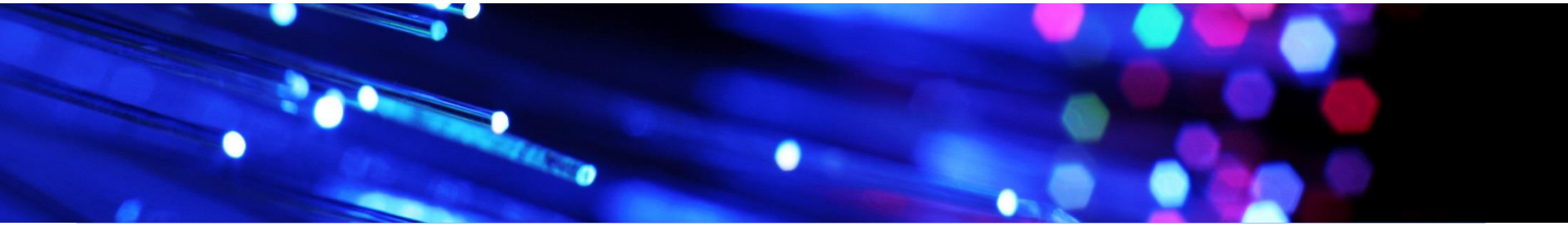
- Spacing set exactly at *B*=330 MHz, without extra spectral guard-bands



Digital signal processing

- Off-line processing experiments. Sampling at 12,5 GS/s with RTO and down-conversion
- Development of DSP algorithms suitable for the FPGA implementation
  - Running at ~600MS/s – sub-band processing
  - Feed-forward adaptive equalizer with 31 complex taps updated by CMA
  - CPE using Viterbi-Viterbi

[1] B. Charbonnier, A. Lebreton, "Demonstration of Low DSP Requirements for FDMA PON", ECOC 2014, P7.4, Cannes, France



Choice of the Forward Error Correction

FABULOUS has a continuous data stream, long FEC allowed

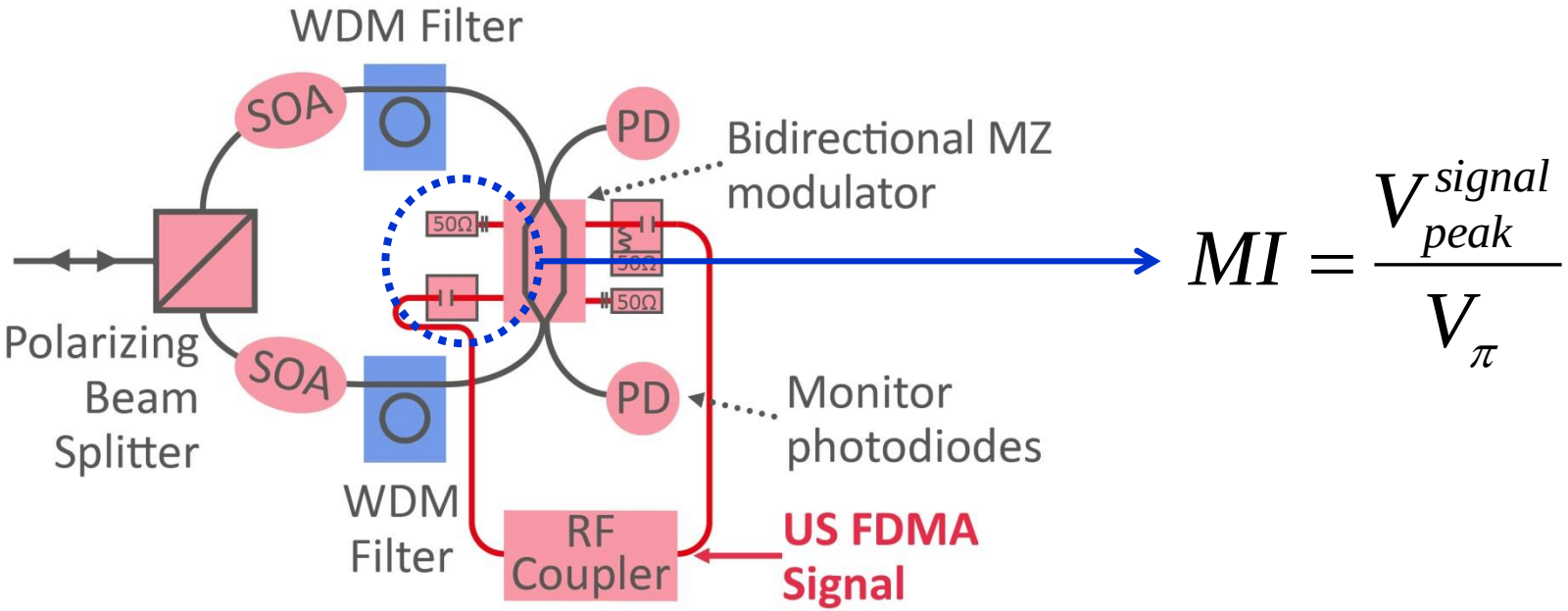
- FEC defined in ITU-T G.975.1 for high bit rate DWDM submarine systems (FEC 1)
- third generation code featuring concatenated FEC with soft decision (FEC 2)

FEC	Code	Overhead	BER pre-FEC threshold
FEC 1	RS(1023,1007) + BCH(2047,1952)	6,69%	$2.17 \cdot 10^{-3}$
FEC 2	RS(992,956) + LDPC(9216,7936)	20,5%	$1.0 \cdot 10^{-2}$

[2] N. Kamiya, S. Shioiri, "Concatenated QC-LDPC and SPC Codes for 100 Gps Ultra Long-Haul Optical Transmission Systems", OFC 2010, San Diego, OThL2.

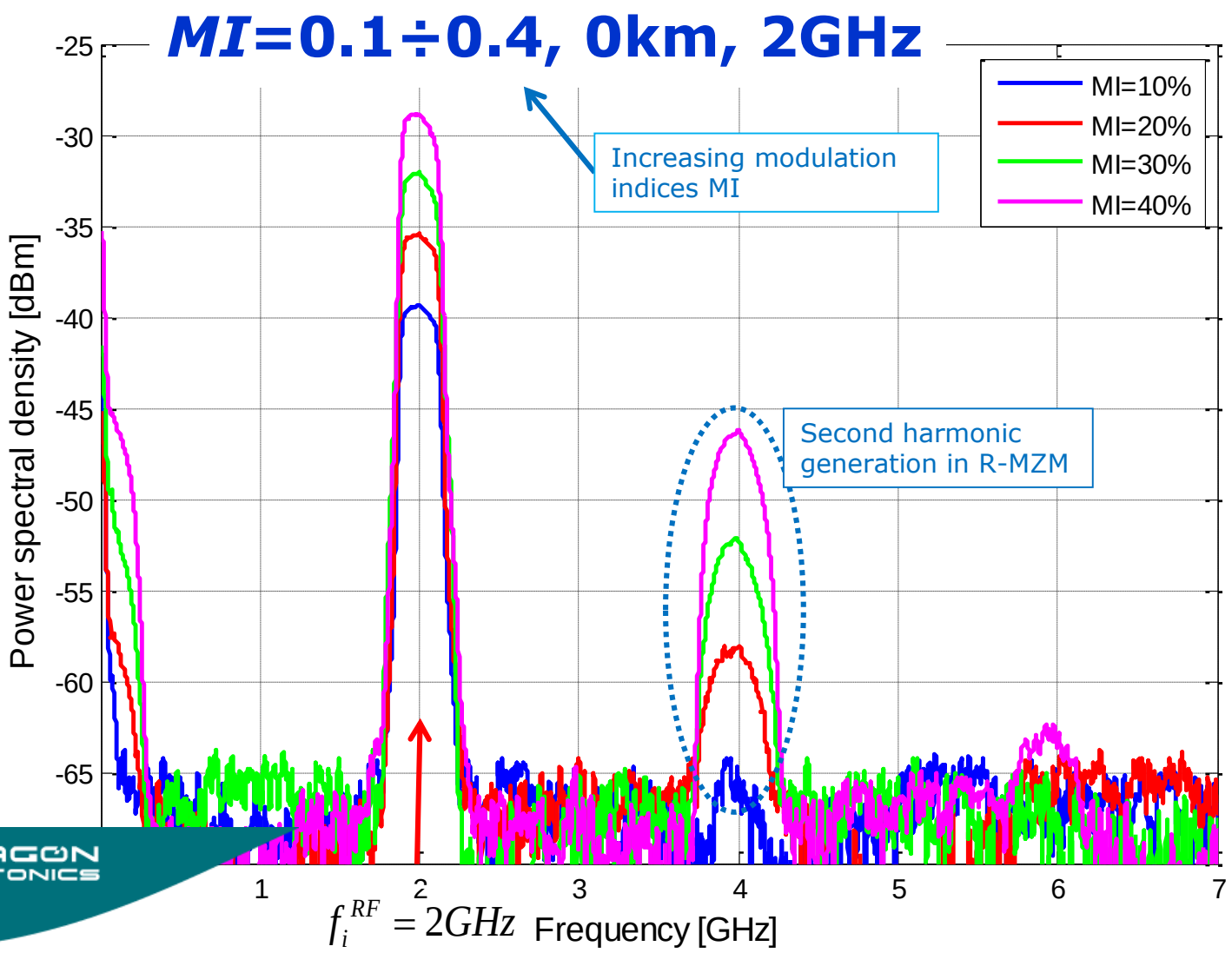
Optimization of modulation index

MODULATION INDEX AT THE ONU TRANSMITTER

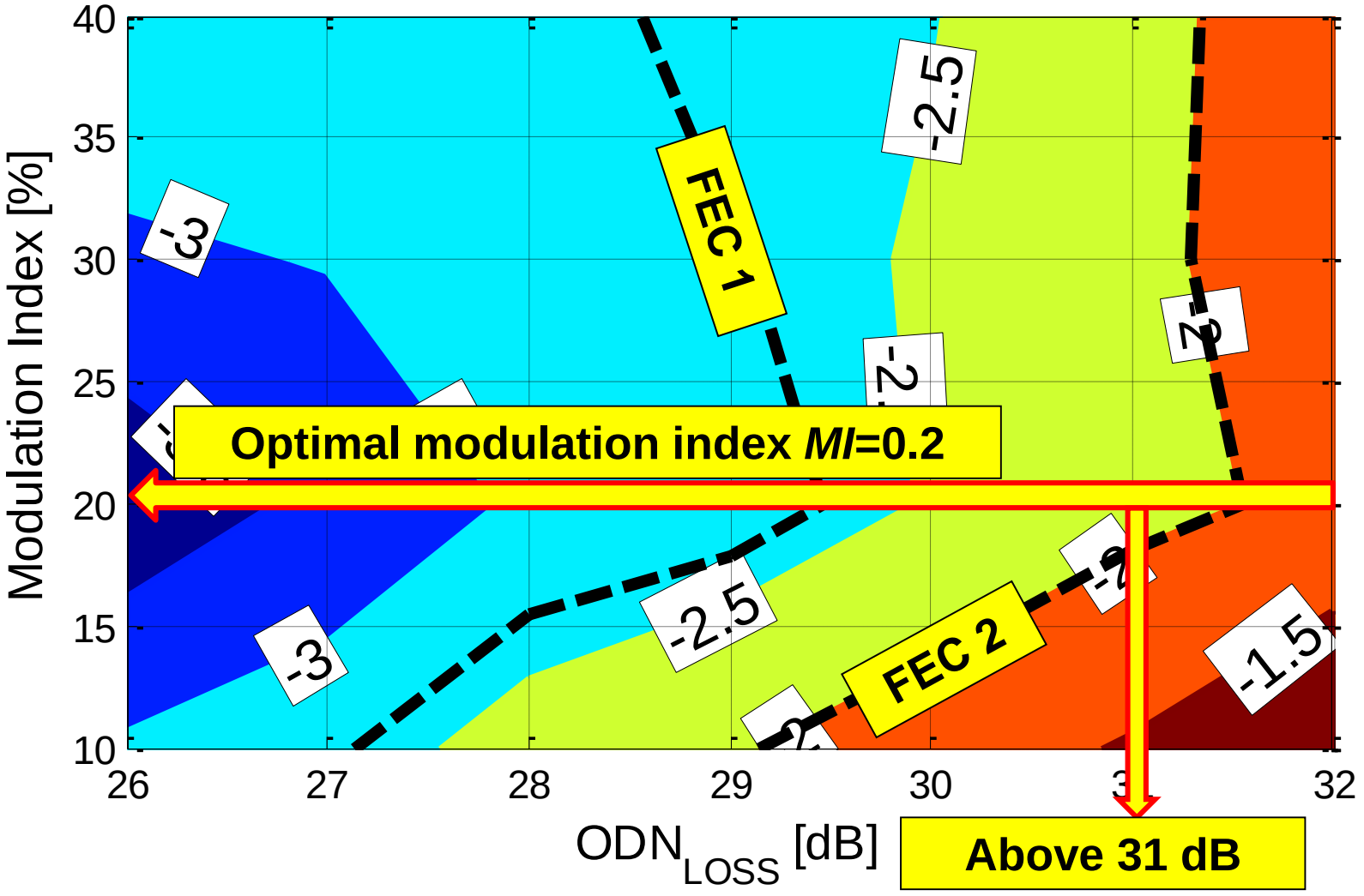


- Small MI: linear behavior but small signal strength
- Large MI: large signal strength but also large nonlinearity

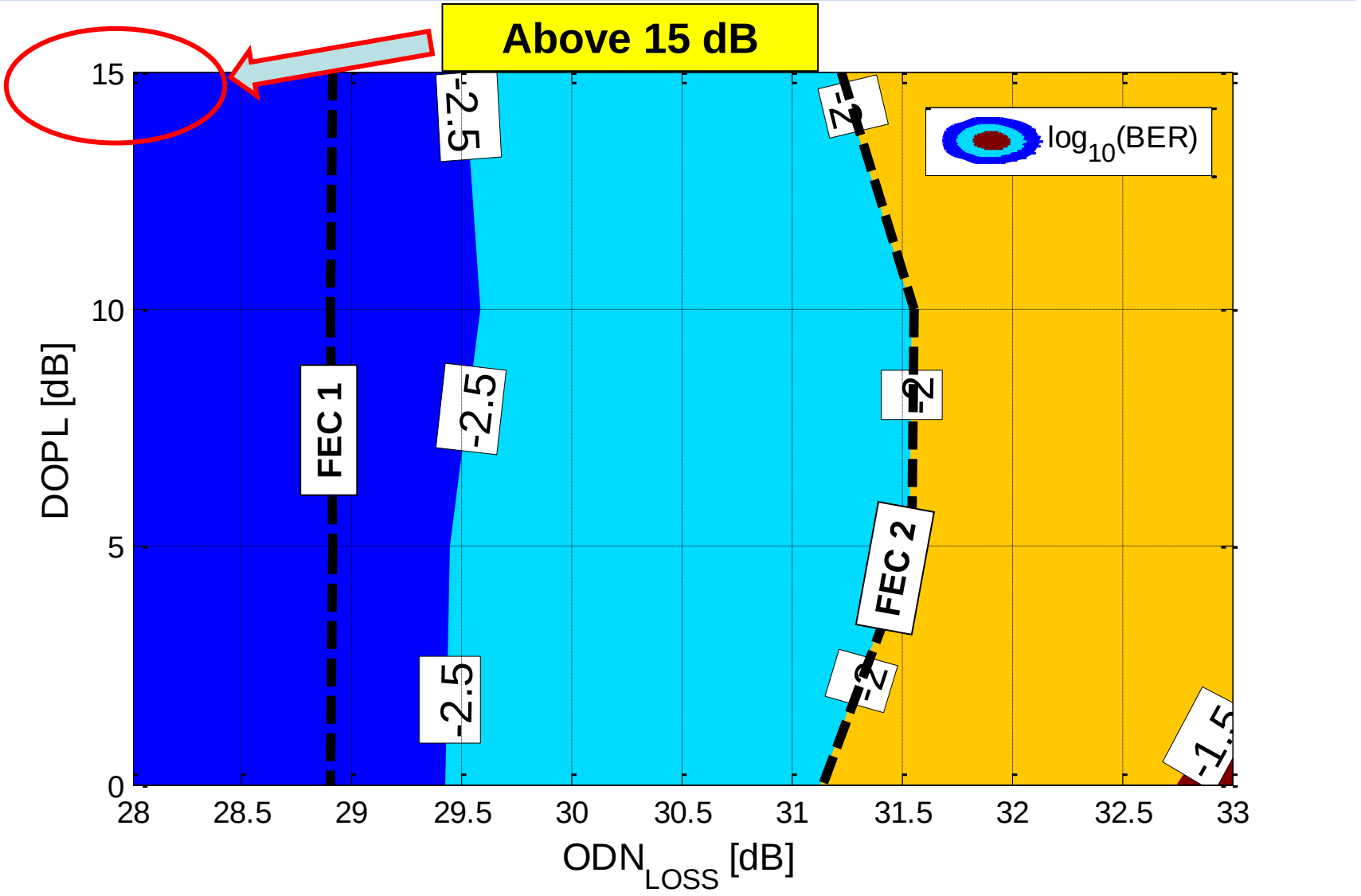
Spectral analysis



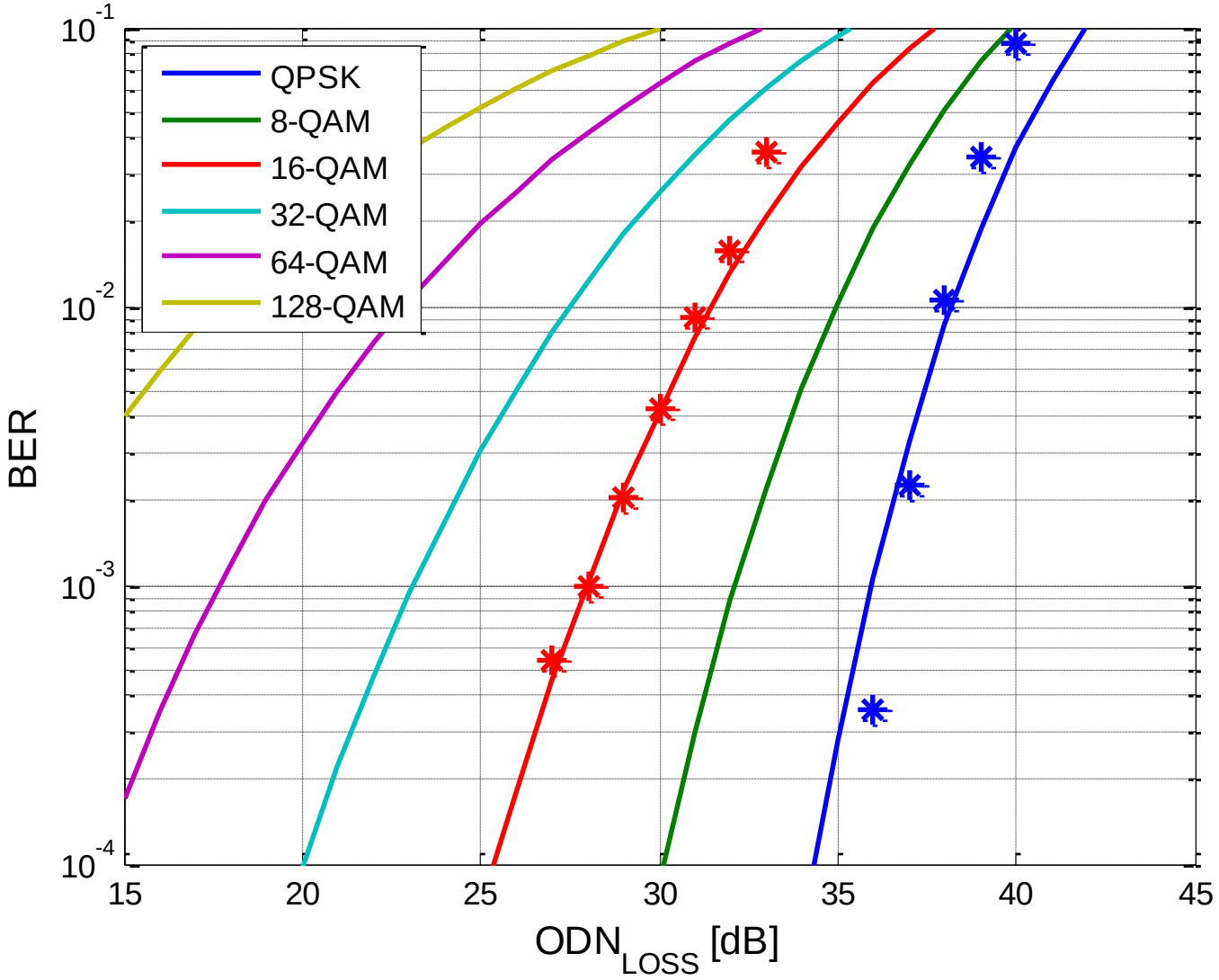
Experimental results with optimized parameters

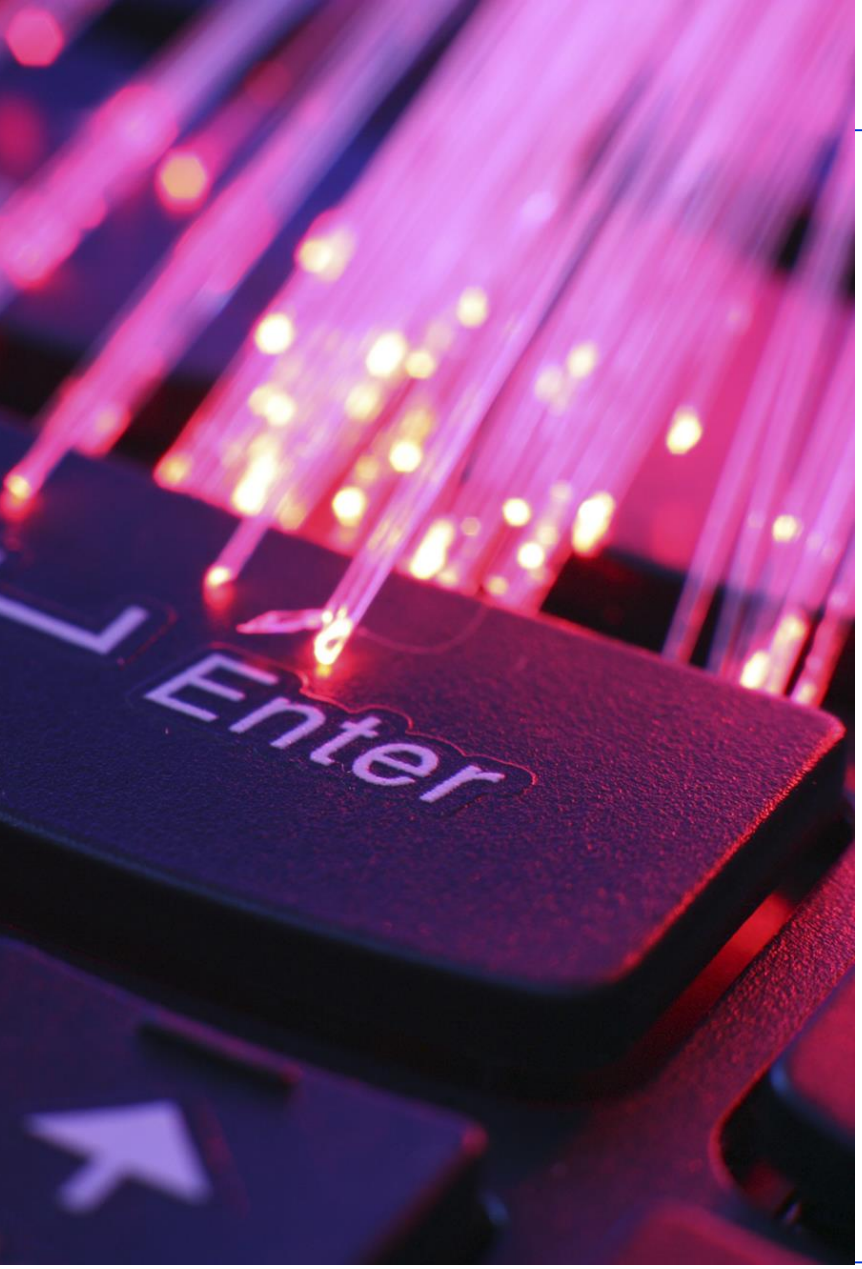


Differential Optical Path Loss



FDMA flexibility – Theory vs. experiments





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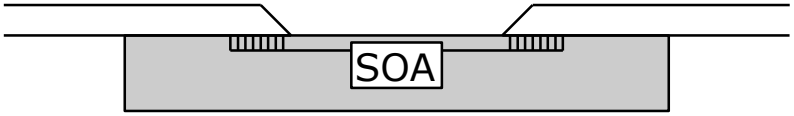
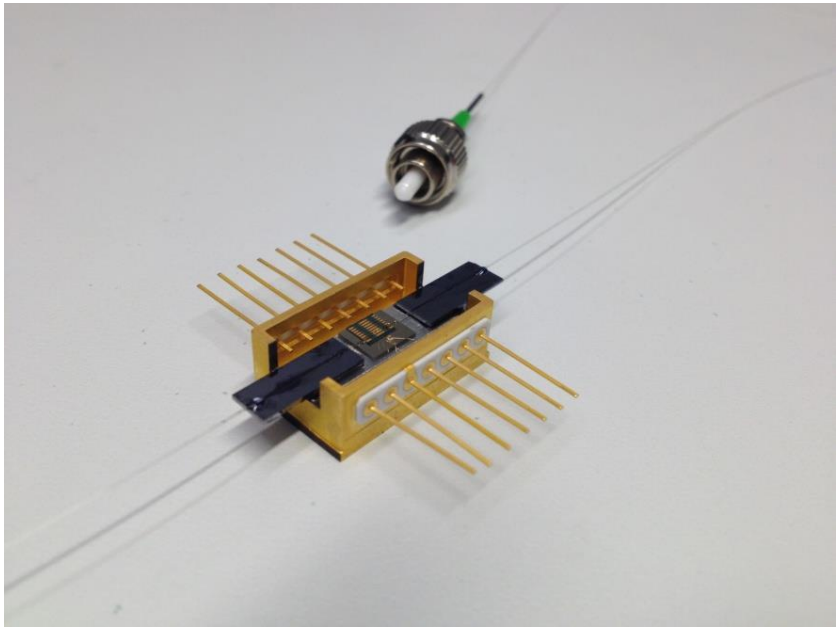
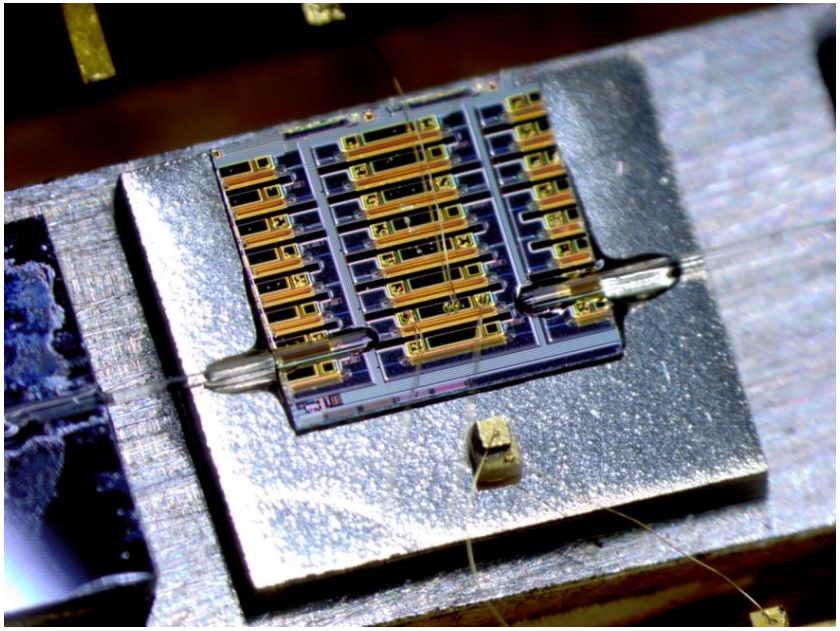
Packaged Hybrid III-V/silicon SOA



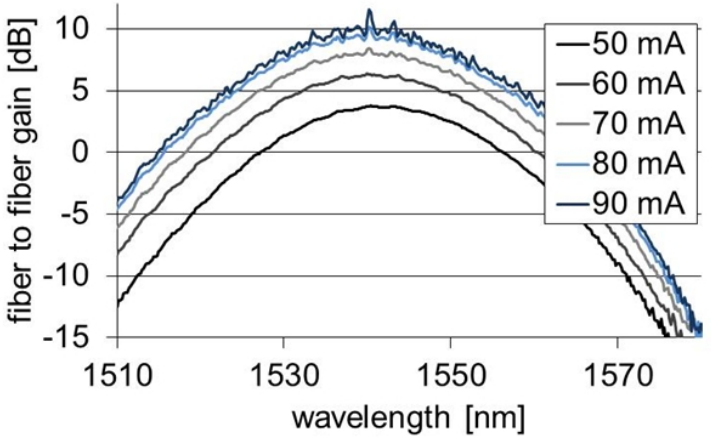




SOA performances

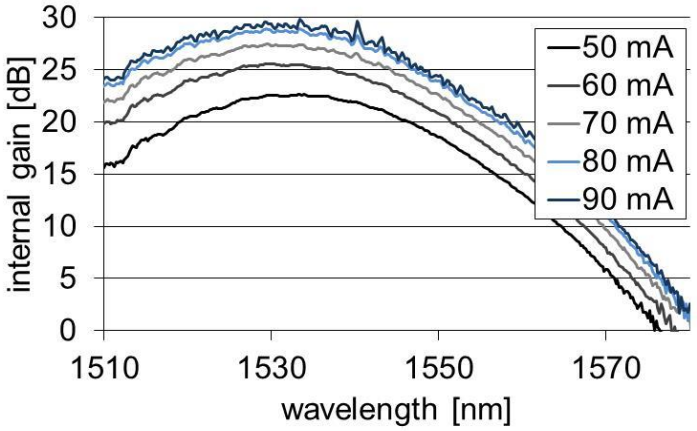
FIBER TO FIBER GAIN

- Up to 10 dB fiber to fiber gain
- Slight blue-shift for increasing current injection



INTERNAL GAIN

- Up to 28±2 dB internal gain
- λ-shift between fiber-to-fiber and internal gain due to grating coupler characteristics

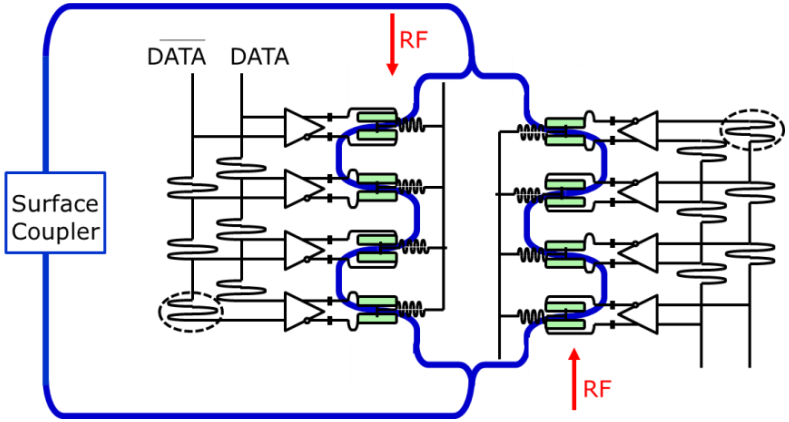


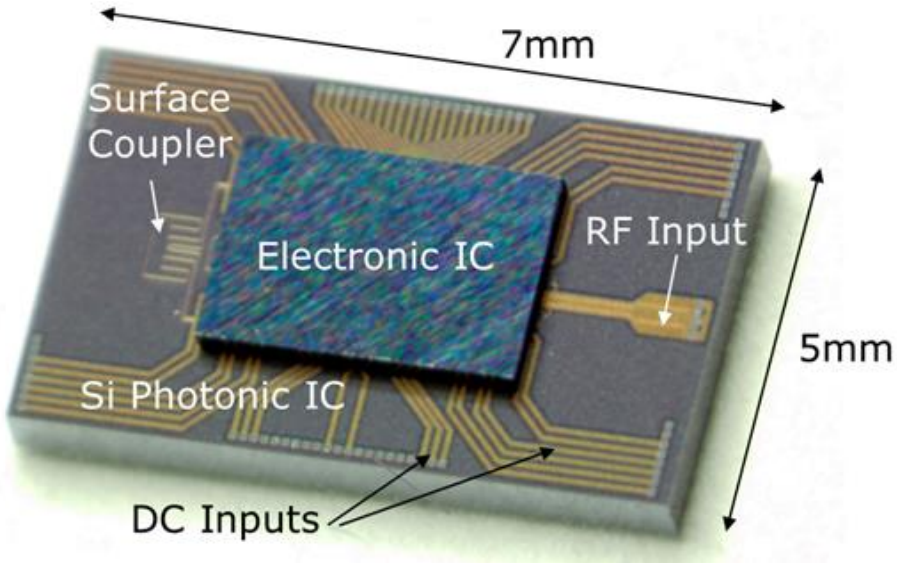
[3] P. Kaspar et al., "Packaged Hybrid III-V/Silicon SOA", ECOC 2014, Cannes, France

Modulator and Driver

Distributed driving architecture

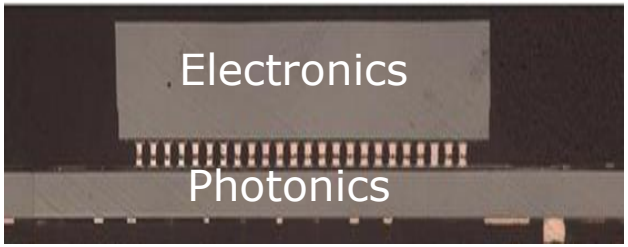
Photonic IC = Silicon Photonics (CEA)
Elec IC = BiCMOS (ST Microelectronics)





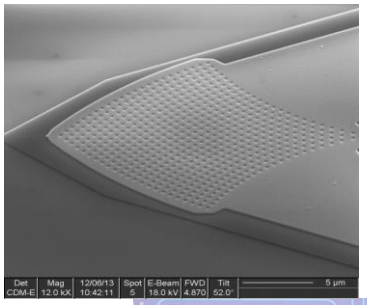
3D integration of Photonic & Electronic ICs

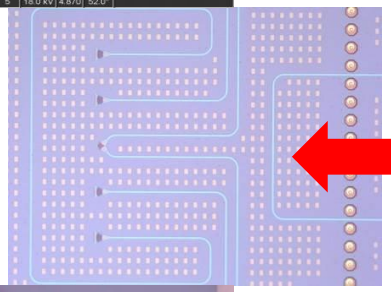
Micro bumps from 3D standard process (CEA)
- ➔ *reduced parasitic capacitance*
- ➔ *Dense interconnections (40µm-pitch)*

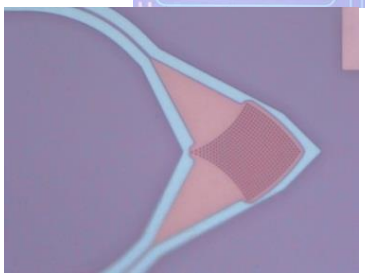


Photonic Integrated Circuit Manufacturing

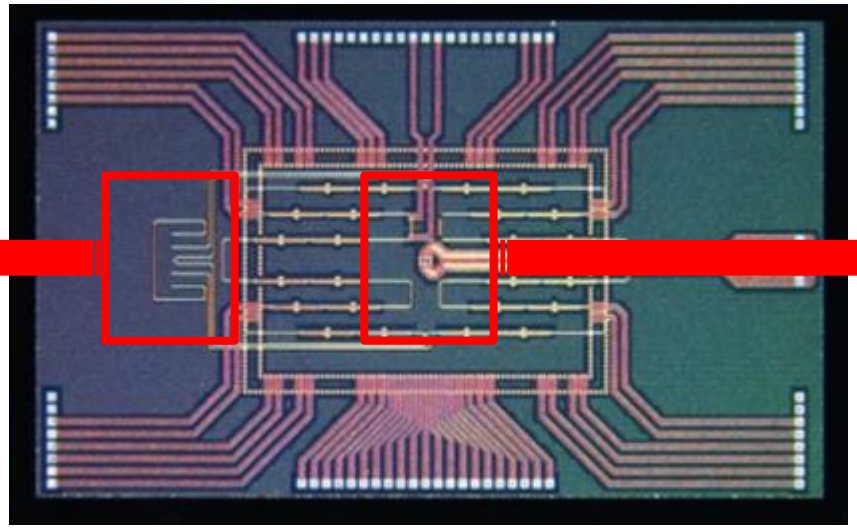
SOI 220nm/2000nm Oxide technology
Processed at Leti on 200mm wafer

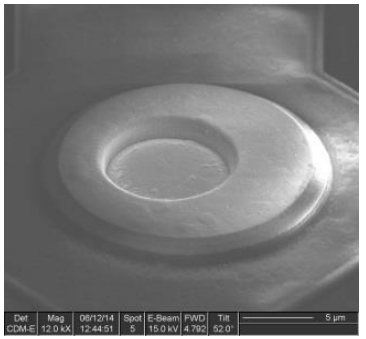


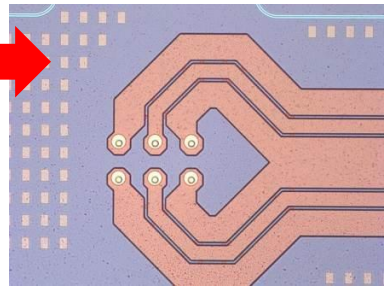




Optical Coupling structures



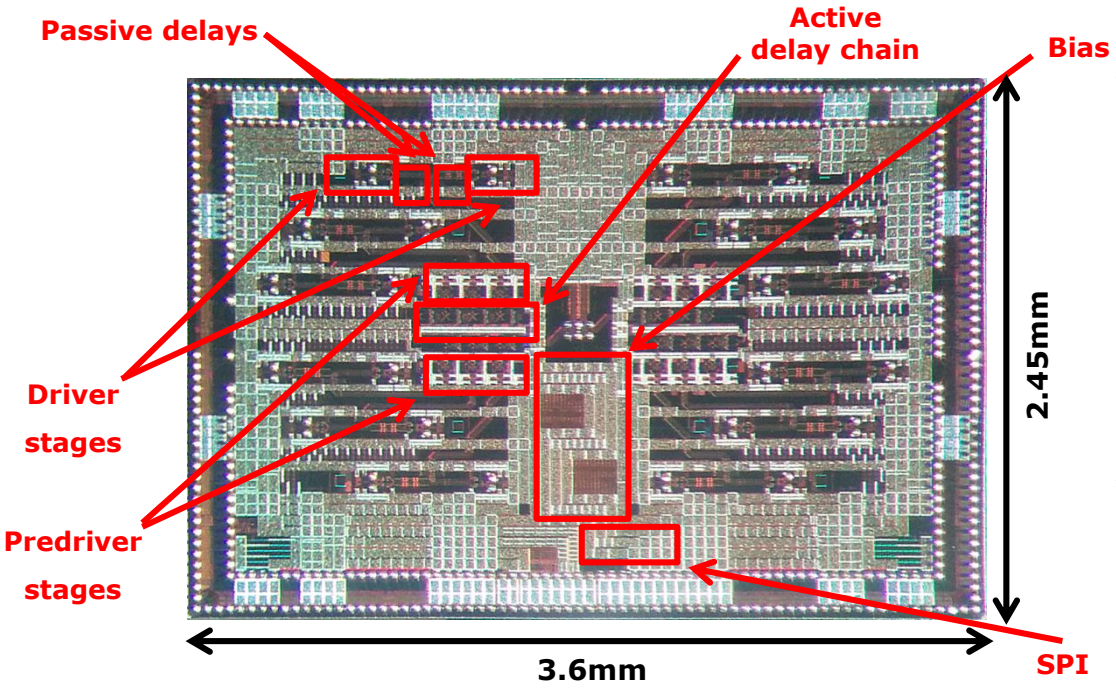




RF electrodes with pads
for bump interconnections

Modulator driver

- MULTISTAGE ARCHITECTURE
  - Minimize impact of integrated transmission line losses
- STANDARD 65NM CMOS TECHNOLOGY
  - 20μm diameter copper pillars



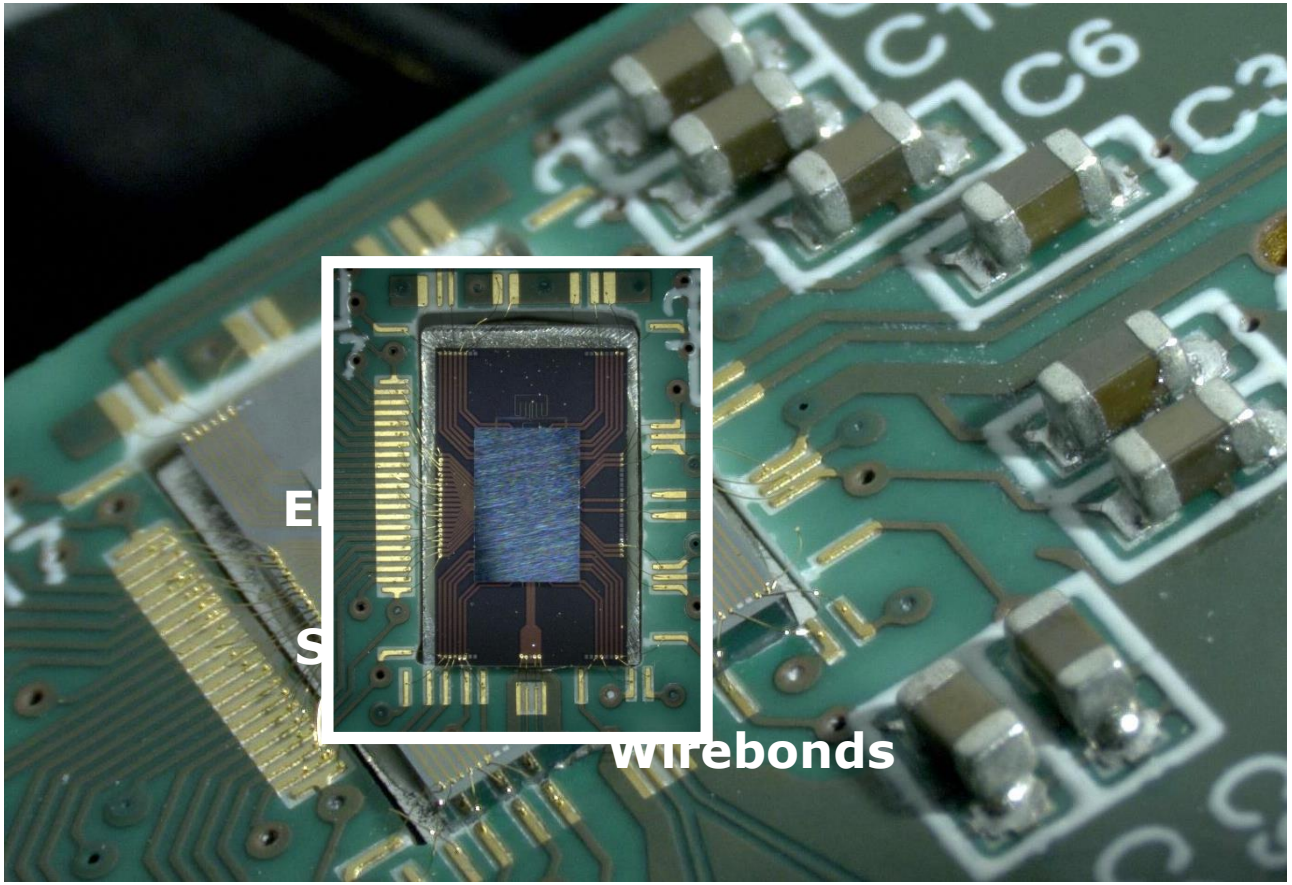
Two symmetrical drivers for co-contra modulation, one per MZM arm

On each MZM arm, 12 CML driver stages

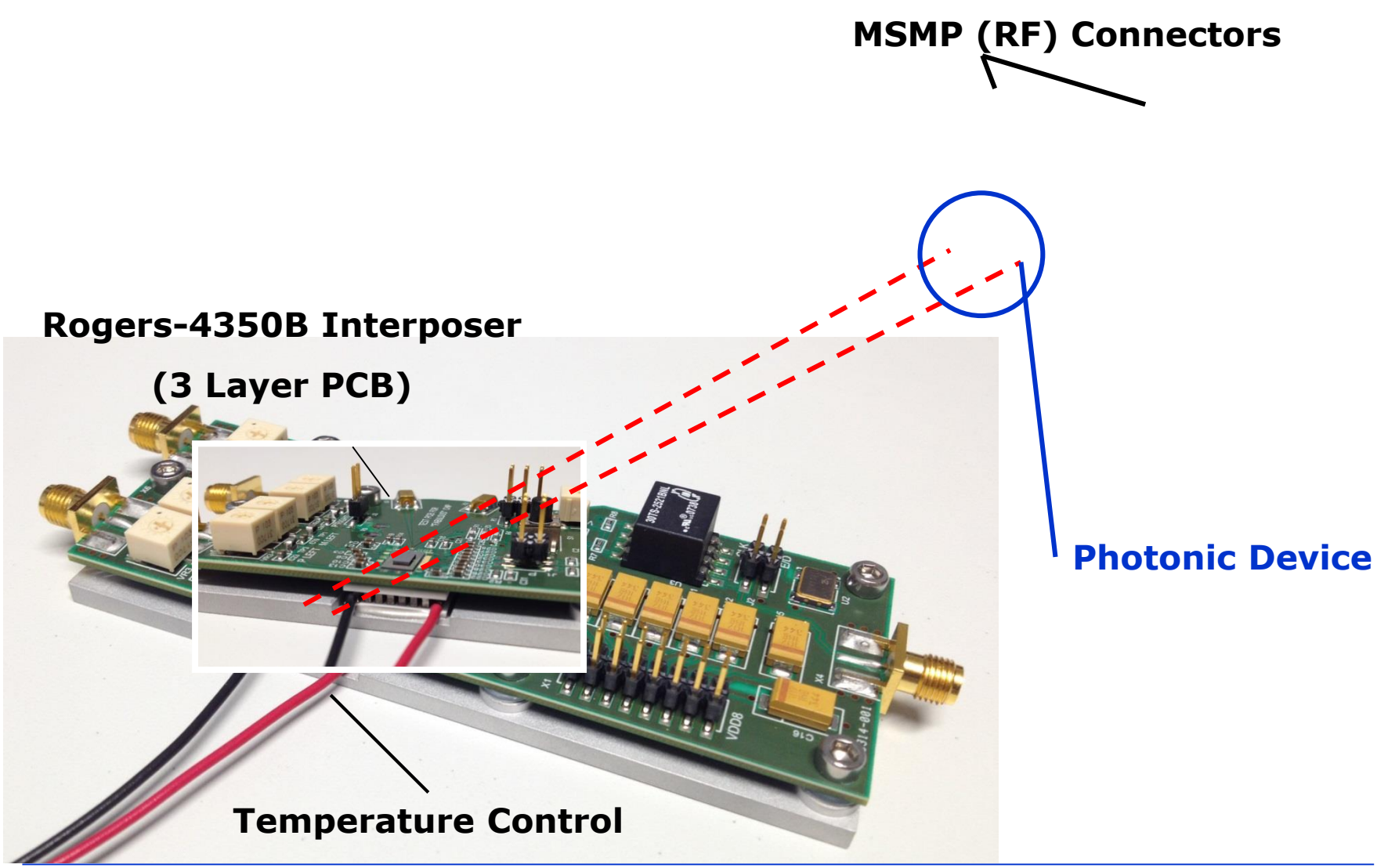
- $1.6V_{ppd}$ driving voltage

Packaging of the ONU

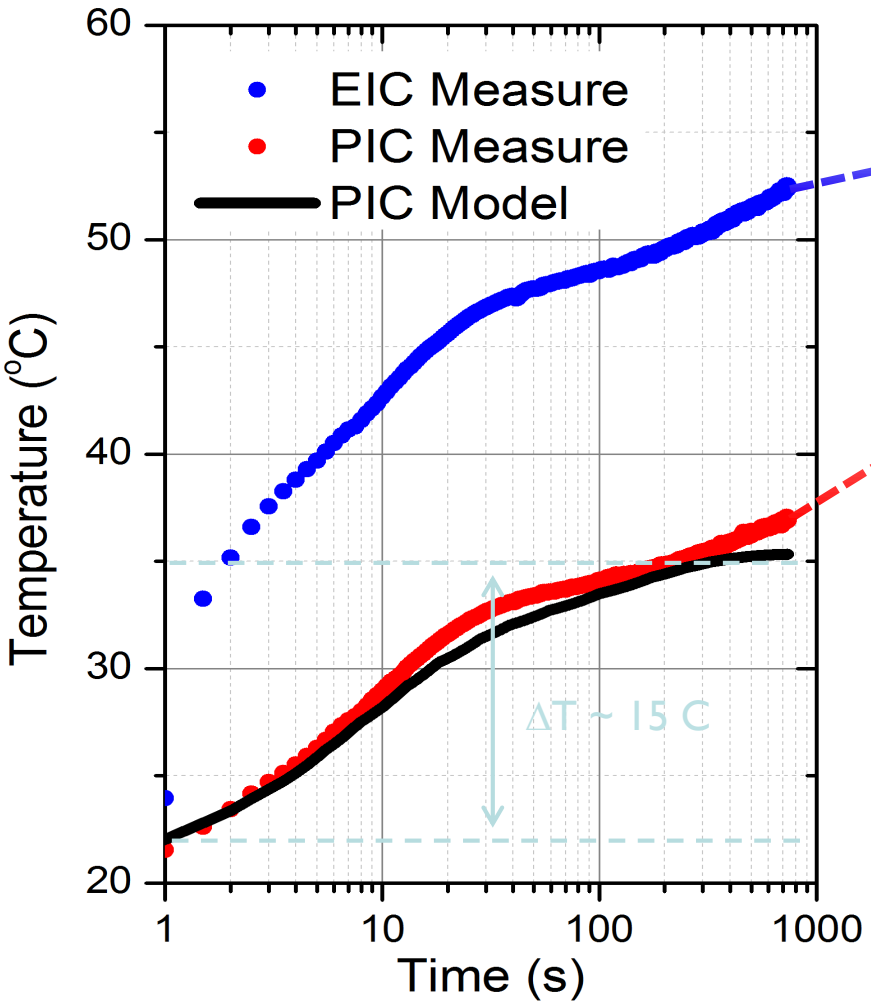
Packaging by Tyndall UCC

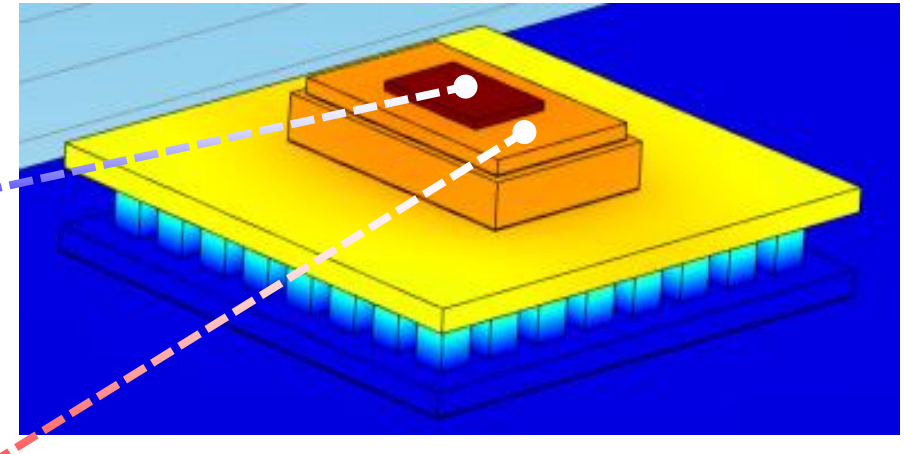


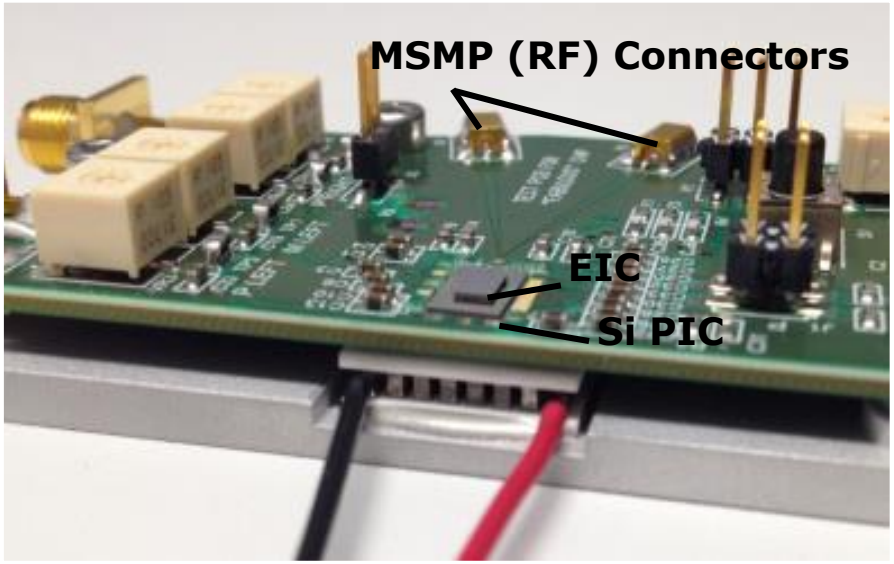
Electronic integration



Thermal effects



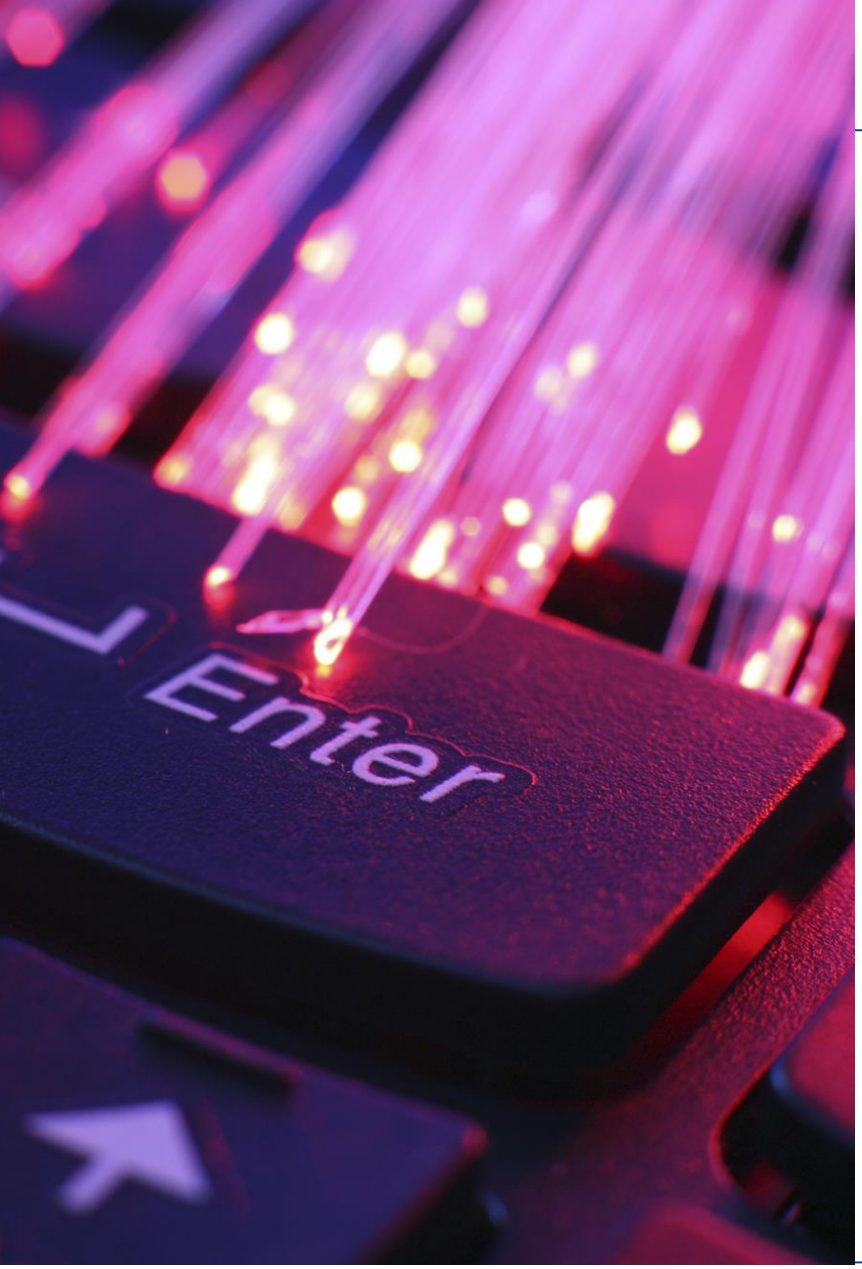




Some commercial data

- We have estimated a power consumption for the SiP integrated ONU of around 8W, of which nearly 5W due to TEC and electrical driver.

- The cost for mass-produced SiP integrated ONUs (1000000 units/year) is estimated <100$. Around 50% is due to packaging.



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We have demonstrated that a FDMA Self-coherent R-PON can serve 32 users with 1 Gbps each, symmetrically, with an ODN loss of 31 dB (ITU-T class N2) and a DOPL of over 15 dB.

The flexibility feature can enable different applications, like coexistence of super-users, such as mobile operators, with other users, or adoption in a vertical-PON scenario for local networking.

We believe SiP can be a key enabling factor for massive deployment of this solution. Will integrated components guarantee the same performances?

Acknowledgments

The research leading to these results has received funding from the European Community's Seventh Framework Programme FP7/2007-2013 under grant agreement n°318704, titled:

FABULOUS: "FDMA Access By Using Low-cost Optical Network Units in Silicon Photonics"

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